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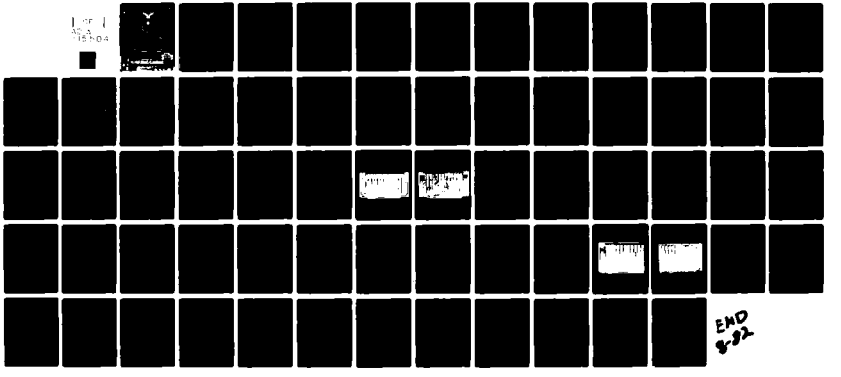

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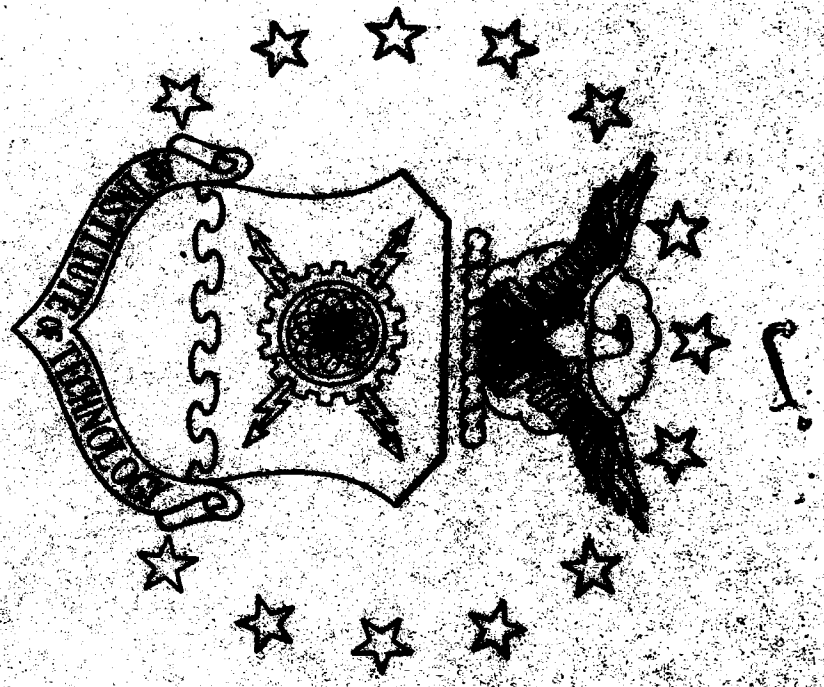

AFIT/GE/EE/81D-40

MICROPROCESSOR CONTROLLED ISOMETRIC CONTRACTIONS OF CAT GASTROCNEMIUS MUSCLE

THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

by

John C. McKeeman, B.S.

Lt USAF

Graduate Electrical Engineering

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PREFACE

I would like to express my gratitude to Dr. J. S. Petrofsky for his extreme patience, technical guidance and understanding during the course of this project. Thanks go to Dr. M. Kabrisky for providing the initial momentum for the project, and for his continuing encouragement throughout the project, especially when times were stormy. Special thanks extend to Harry H. Heaton and Debbie Hendershot for the photography and cat surgery, respectively.

My deepest gratitude is extended to my wife for her love, loyalty and understanding without which this project could not have been completed.

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Abstract

Increasing numbers of spinal cord injury victims due to automobile accidents , sports injuries and gunshot wounds reflect a growing need for a paralysis cure. One method under study to alleviate the plight of spinal cord injury victims is the use of microcomputers to control the stimulation of the remaining motor nerve. If the motor nerve is intact and is carefully stimulated, muscle contraction will occur. Coordinated contraction of two or more opposing muscles can produce limb movement and using small, fast microcomputers to control the stimulation of the muscle tissue, and hence movement, a possible cure to the paraplegic problem nay be found.

The object of this project was to produce controlled fatiguing muscle contractions in the gastrocnemius muscle of cats. The composition of the muscle tissue is identical to man's and controlled contractions in the cat will lead to the same contractions in man. In order to produce an accurately controlled contraction, first a computer system was constructed from an Intel 8085 micmoprocessor. Next,controllable stimulators for the motor nerves were constructed and controlled by the microprocessor via digital to analog convertors. Feedback from the muscle under test was then interpreted throughanalog to digital convertors, such that the microprocessor controlled the contraction tension of the muscle as a constant. Through the feedback, the processor was able to induce highly accurate sustained muscle contractions and with the high speed of the system, future multi-muscle control systems could develop. This would allow limb movement in previously unusable limbs.and pave the way for future solutions to the paraplegic problem.

I. Introduction

Background

Each year thousands of incurable spinal injuries occur from auto accidents, sports injuries and gunshot wounds (Smart and Saunders, 1976). At the turn of the century, a victim of such an injury stood very little chance of survival, as the lack of antibiotics and spinal shock treatment almost assured death in the first three years after injury. Although today's technology has lengthened the expected life span of a spinal injury victim, no "cure" has been found to completely alleviate the muscle paralysis of a spinal injury victim.

Research to aid in the plight of spinal injury victims, stems into many directions. The four major branches of this research are; alternate forms of mobility, reconstruction of the damaged spinal cord, direct muscle stimulation to provide limb movement and stimulation of muscle motor nerve. Although the last three branches of research might offer a future cure of paralysis of the spinal injury victim, the first branch does not attack the problem itself and only offers a temporary solution to the victim's immobility.

Several types of alternate mobility forms have been tested to aid paraplegics and quadraplegics. One device of this type of solution is a large metal frame which surrounds the operator. The frame is completely controllable by the operator by way of hydraulic levers and motors and can move the operator over a limited expanse (Townsend and Vepofsky, 1976). The major drawback to this type of device is the fact that, in addition to the bulkiness of the apparatus, large quantities of power are needed from the internal batteries of the device in order for operation. Again,

even if the size and power requirements of such a device were trimmed to produce a fairly feasible model, the question of making paralyzed limbs move by their controlling musculature has not been addressed.

A second approach to the paralysis cure, is direct stimulation of the muscle tissue to provide proportional control of the appendages, and restore stability to the joints (Peckham, 1976; Petofsky, 1978). Initially it was thought that the muscles could be stimulated to contract by the use of skin electrodes (Milner, 1970). The problems caused by this were that the very high currents needed to induce contraction often caused irritation and burning of the skin (Scott, 1968). By utilizing intramuscular electrodes for the stimulation, slightly lower voltages and currents were used without the burning effect of the skin electrodes (Scott, 1968). The major problems with this type of cure of paralysis stem from the high power requirements. The objective of a total cure for paralysis is to manufacture a device that is small enough to be worn or carried without notice. Power for the intramuscular electrode type of stimulation would require a large power source too bulky to be carried. Lastly, muscle movement during contraction makes it very hard to keep electrodes in place for extended periods of time (Peckham, 1976). When this problem along with the power requirement problem are solved, this method of muscle control might be a feasible solution to the paralysis problem.

The third branch of research for paralysis centers around the damaged spinal cord itself. At the Russian Polenov Neurosurgery Research Institute, much work has been done on rejuvenation of the damaged nerve by injection of hyaluronidase, a tissue softening enzyme. The principle of the tissue softening enzyme is that the scar tissue around the damaged spinal cord will

be broken down, thereby encouraging regrowth of the healthy nerve fibers and transmittance of nerve signals (Matinyan, 1976). Results from the Russian's work have not been duplicated in the United States, thereby raising doubt on the work done. Other work in this area includes the work of United States scientists formulating an electronic bridge around the damaged area. Technology at the present time is not adequte to ensure this type of paralysis solution in the near future.

The last area of research in the paralysis solution revolves around the hypothesis that stimulation of the remaining muscle motor nerves can induce muscle contraction and limb movement (Petrofsky, 1978; Solomenow, 1978). In a spinal injury most of the motor nerves will still be intact below the area of injury. By stimulating these nerves with pulses of amplitude less than one volt, the muscles can be made to contract (Petrofsky, 1978). Use of present day computer technology would enable small, portable computers, stimulators and feedback channels to control co-ordinated movement of muscles and limbs. While this research is not completed, work is still being done by Petrofsky et al. at Wright State University. The thrust of this project would be to advance the work done at Wright State University by observing the use of state-of-the-art technology computers on the stimulation of muscle tissue through motor nerves.

Objectives

The objectives of this project were two fold. First, a method was sought by which muscle contraction could be artificially and accurately controlled by a computer. Second, the method for controlling the muscle was to be opitimized so that future multi-muscle stimulations could be controlled from a single computer system.

If completed, the data from this project would help to further the paralysis research currently being done at Wright State University in many ways. In order for a limb to achieve co-ordination, several muscles must be finely controlled simultaneously. A new computer controller utilizing state-of-the-art technology would allow much quicker response to muscle feedback. Therefore, the several muscles needed for movement could be stimulated much more "simultaneously" and with greater accuracy than with older technology computers. This then would pave the way for computer control of all muscles necessary for co-ordinated leg movement.

Approach

To complete the objectives outlined above, the following approach was used. First, research was done to determine what equipment would be required to stimulate the medial gastrocnemius of a cat. Next, each piece of equipment was constructed and tested to ensure proper functioning. Finally, the test equipment was assembled into one unit and used in conjunction with an anesthetized animal to validate its operation.

The equipment which was deemed necessary to obtain the data was a small, but fast computer system, two channels of both analog to digital and digital to analog-controlled voltage controlled stimulators. A state-of-the-art Intel 8085 microcomputer was chosen to control the stimulations since it operates quickly (3 MHz clock) and requires few support chips. In addition to these reasons, the 8085 requires few software modifications from existing programs for computer control of movement which have been developed around an Intel 8080A microprocessor, since the software is completely upwards compatible.

Figure 1 outlines the experimentation needed to completely test the computer controlled stimulation of the gastrocnemius muscle. First, the muscle is stimulated with a tetanizing frequency pulse to determine the value of the maximum tension developed. This value is multiplied by the percentage of tension desired in the isometric contraction, and is called the target tension of the contraction. The target set potentiometer is then manually set so that the output of the analog to digital converter corresponds to the tension desired. After a stimulation pulse set is released, the outputs of both analog to digital converters is sampled. If a difference is noted between the digitized outputs of the target and the actual tension developed, the computer adjusts the stimulators accordingly to correct the difference.

The stimulators used on the motor nerves of the muscle are controlled by the microprocessor through the digital to analog converters. After each sampling of the strain gauge output, the microprocessor sends digitized information to the correct digital to analog converters to adjust the pulse width or amplitude of the stimulation pulses. Each D/A converter is assigned as an output port in the microprocessor, and it is through these ports that the correct digitized information is passed to the correct D/A converter.

After each of the above pieces of equipment were constructed, each was tested to verify its function. Via the computer S-100 bus, all of the pieces were interconnected and tested to ensure the unit functioned. The last stage of the testing involved subjecting an anesthetized animal to computer stimulation and collecting the raw data. The actual experimentation consisted of stimulating the nerves at a rate and amplitude to ensure that the muscle maintained a constant tension on the bar until complete fatigue was reached.

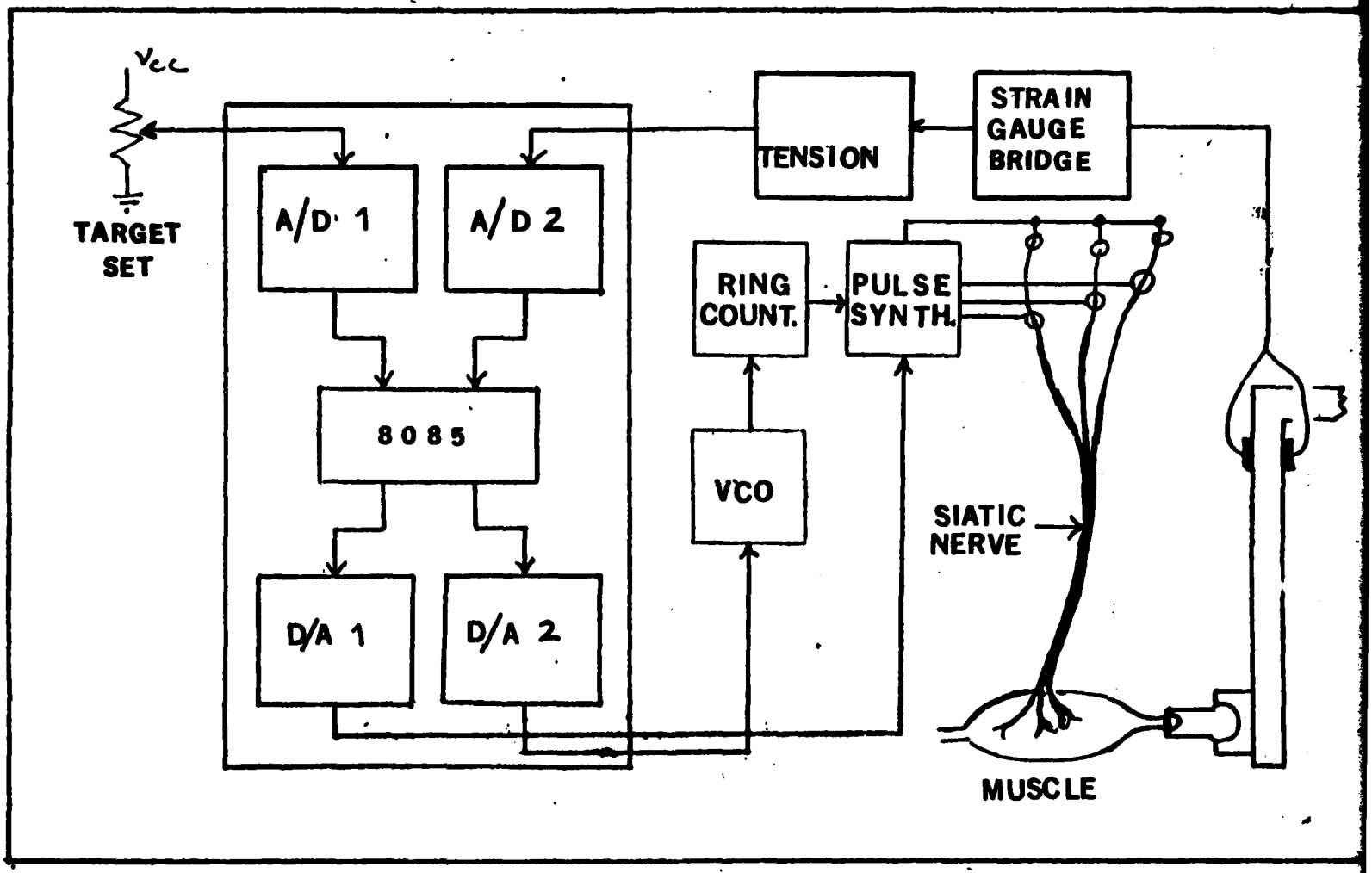


FIGURE 1. OVERVIEW OF EXPERIMENT

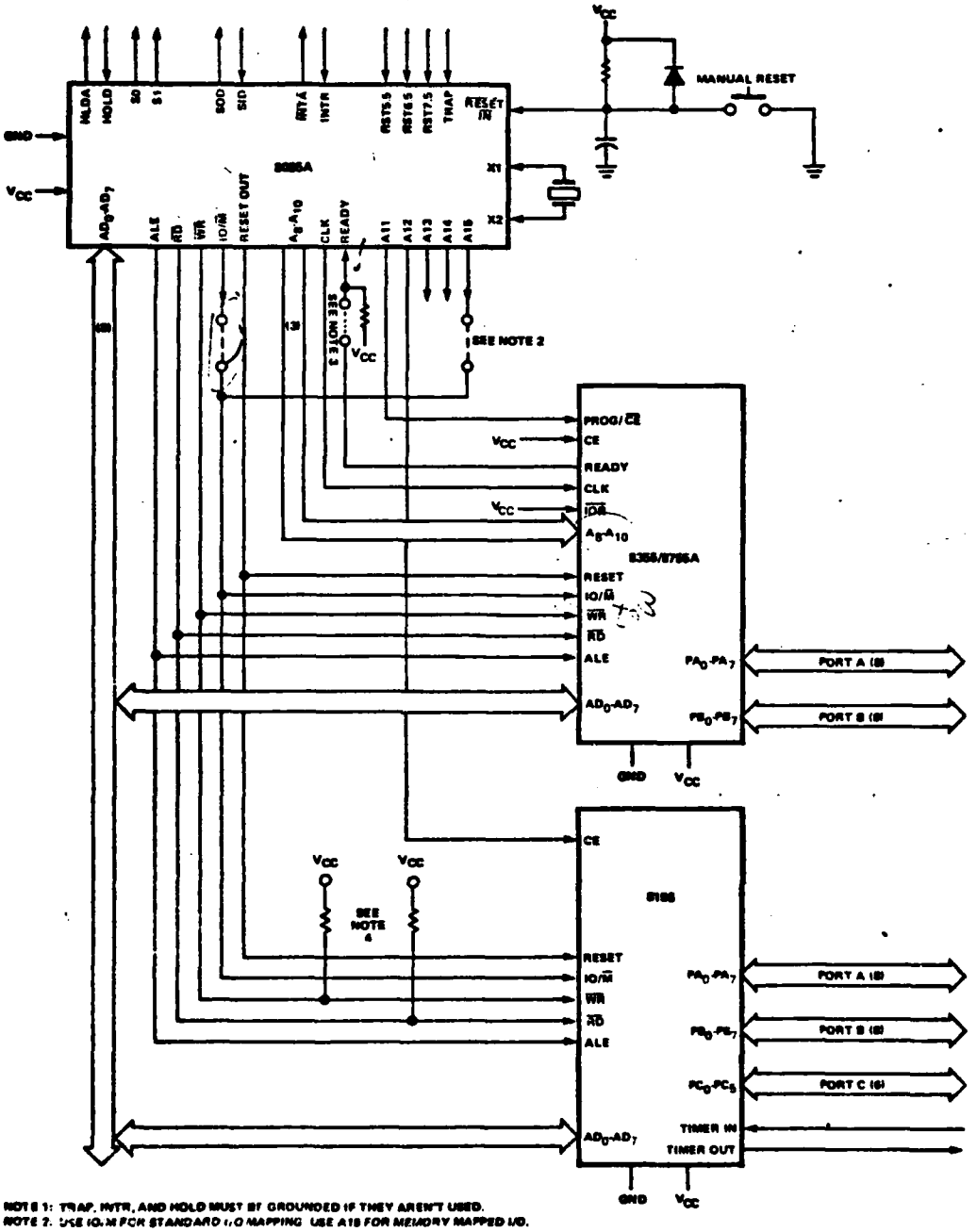
II. The Intel 8085 System

Once an Intel 8085 microcomputer was chosen as the basis for the project, research followed to determine what steps would be needed to construct a complete system. The steps in building the system would require: an S-100 motherboard, an 8085 system that was S-100 compatible, a peripheral interface, and a system software initialization necessary to bring the entire system up. If built and tested in sequence, a working microcomputer system would result.

The S-100 Bus and Computer Mainframe

For the central processing unit to communicate with the external memory, I/O ports and external devices, a method for this type of high speed communication is the S-100 bus. Each printed circuit card holding the CPU, the memory or the device, has one hundred etched "pins" on one edge of the card. The pins are arranged so that fifty appear on each side of one edge of the printed circuit card and are spaced 0.125 inches apart. Each pin is assigned to carry a single line of information to or from the card, and this is an industry standard. Because the S-100 bus is almost universally accepted, a very flexible computer system can be constructed allowing almost any other type of peripheral board to be added to the system. It was for this reason that an S-100 type bus was chosen for the project system.

The etched edge of the card that contains the 100 bus lines is plugged into a 100-contact connector. This connector, called an edge connector, transforms the 100-vertical bus lines of the card into 100 parallel horizontal pins for the S-100 bus mainframe. Each edge connector pin is then soldered into place onto a printed circuit board called the mother board.



NOTE 1: TRAP, INTR, AND HOLD MUST BE GROUNDED IF THEY AREN'T USED.
NOTE 2: USE IO/M FOR STANDARD I/O MAPPING. USE A15 FOR MEMORY MAPPED I/O.
NOTE 3. CONNECTION IS NECESSARY ONLY IF ONE T_{WAIT} STATE IS DESIRED.
NOTE 4. PULL UP RESISTORS RECOMMENDED TO AVOID SPURIOUS SELECTION WHEN $\overline{RD}$ AND $\overline{WR}$ ARE 3-STATED. THESE RESISTORS ARE NOT INCLUDED ON THE PC BOARD LAYOUT OF FIGURE 3-7.

FIGURE 3-6 MINIMUM 8085 SYSTEM

FIGURE 2. INTEL 8085 SYSTEM

The mother board is a printed circuit board which links the 100 pins of any plug in card to all others through the edge connectors. Consisting of 100 parallel lines running the length of the board, the mother board acquired for the project contained room for 22 edge connectors or 22 separate plug-in cards. After being outfitted with hardware from a local source, the board was completed except for power supplies for the ±12V and five volt lines.

Regulated power supplies were built for the ±12V lines. Output of the regulators was boosted by the use of two 2N2055 power transistors to provide up to seven amps current at full load. The five-volt power supply was purchased to produce up to 12 amps current for the system. After being connected to the mother board, the power supplies were successfully tested for proper voltage values. The final step in constructing the mother board was to check all S-100 lines to ensure that two or more were not shorted. After this was completed, the S-100 bus mainframe was mounted into the computer case and deemed ready for use.

Creation of Intel 8080 Compatibility

Once the 8085 central processing unit was developed, it was incompatible with the 8080 S-100 bus system. Therefore, major additions to the 8085 circuitry were needed to allow the 8085 CPU to run on the 8080 bus. These additions fell into five categories:

1) Demultiplexing of the address/data lines.
2) Separation of the data in/data out lines.
3) Creation of 8080 command/control lines.
4) Creation of 8080 equivalent status lines.
5) Generation of 8080 timing signals.

Demultiplexing of the Address/Data Lines

The lower eight bits of address and the eight data bits are multiplexed on the same eight lines from the 8085, therefore, they must be separated or demultiplexed before being used. Demultiplexing of the lower eight bits of address from the data lines was easily accomplished as shown in Figure 3. Each address/data line was first buffered through continuous output buffers (8T97S) then fed into eight bit output port, an Intel 8212. With the device selection pins $\overline{DS_1}$ and DS_2 wired directly to ground and Ale, respectively, the 8212 is a direct output for the lower eight bits of address at the beginning of each machine cycle. For the remainder of the cycle, the 8212 is a data batch for the address lines. Reset out connected to $\overline{Clr}$ clears the output each time the 8085 CPU is reset. Address disable, ($\overline{ADDDSBL}$), tied to the mode input allows the 8212 to continue normal operation until the mode input is driven low. When mode is low, all outputs are tri-stated or put into high impedance states, allowing external devices to have control of the address bus. The enable inputs of the buffers for $A_8 - A_{15}$ are also connected to address disable, which when driven low drives the enable inputs high, tri-stating the outputs or address lines.

Separation of the Data In/Data Out Lines

Separation of the data in/data out lines was complex, as many factors had to be taken into consideration. Five separate signals determine whether data will be inputted, while two signals control the output of data. Starting with the data input, data on the input bus lines will only be inputted to the CPU under the following condition:

$$\overline{INPUT\ DATA} = \overline{SSWDBLE} + \overline{RD} - \overline{HDA} + \overline{SS} - \overline{RUN}$$

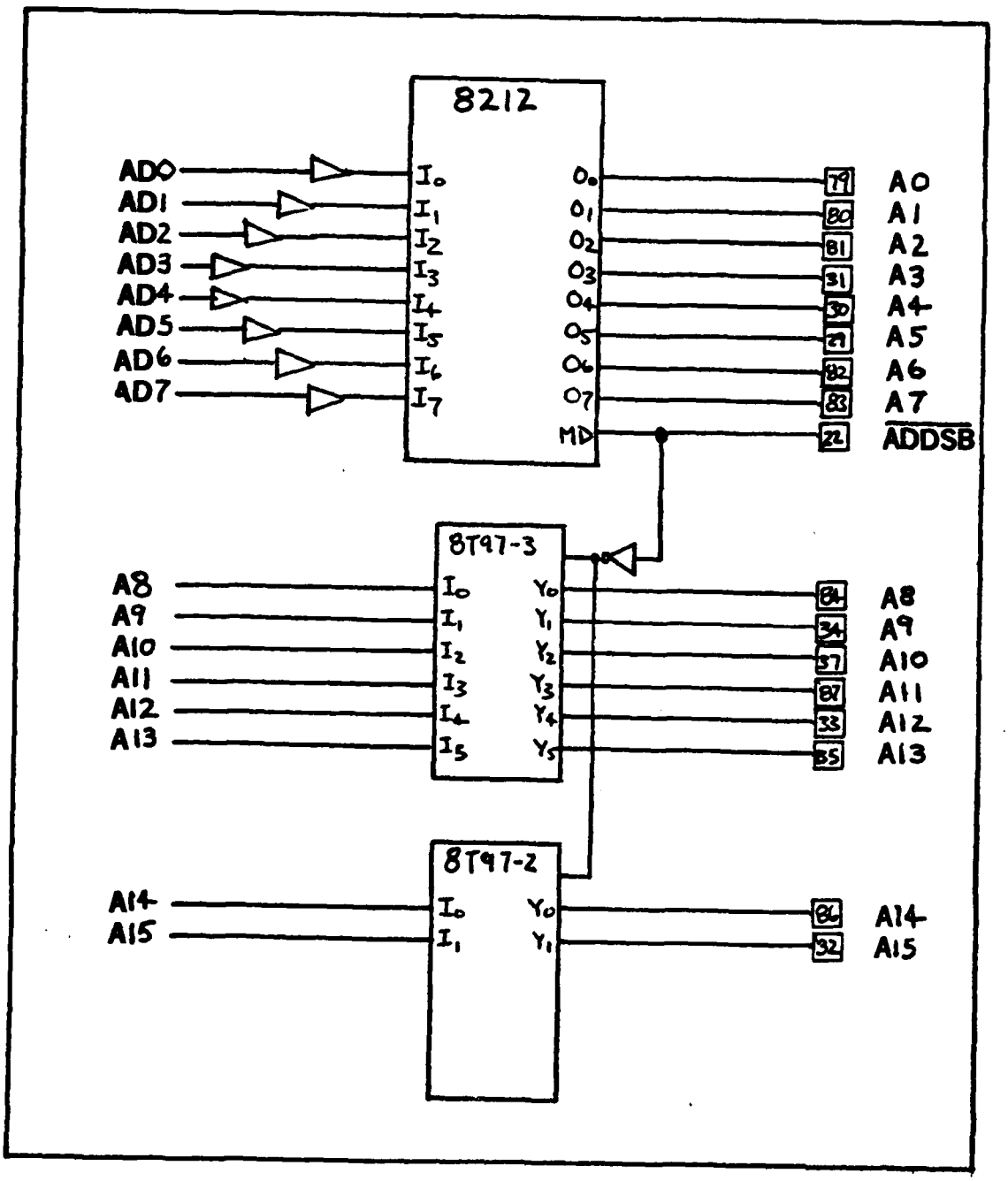


FIGURE 3. ADDRESS LINES

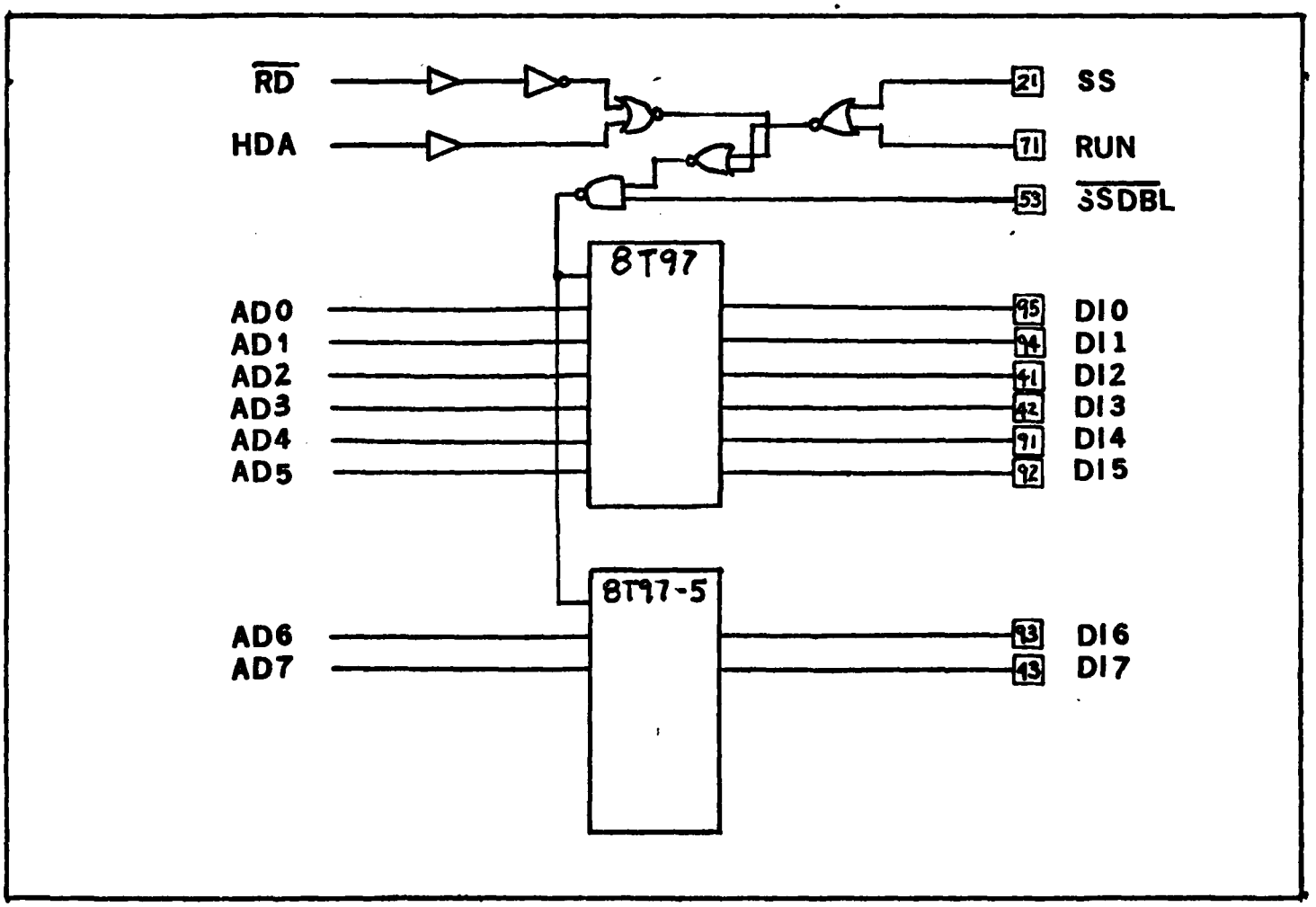


FIGURE 4. DATA INPUT

Since switch disable is abbreviated with SSWDBL, while RD is read, HDA is hold acknowledge, SS is single step, and RUN is run. The gating will achieve the input condition as shown in Figure 4. At all other times, the chips are not enable, and the outputs are in the high impedance mode.

Data output occurs as a function of two variables, write output (WR) and data out disable (DOD). The 8085 issues a $\overline{WR}$, which is active low when data is to be written out, which the DOD is an active input high from external devices to free the data lines. By grading these in an OR gate, the 8T79 buffers only put data on the data lines when both $\overline{WR}$ and DOD are low.

Creation of 8080 Command/Control Lines

The creation of 8080 equivalent command/control lines was completed by simply gating and buffering existing 8085 signals as shown in Figure 6. Output of the 8797 buffers was controlled by the command output disable input, active low. When the command output disable is drawn low by peripheral devices, the command outputs are all tri-stated.

Creation of 8080 Equivalent Status Line

Status outputs reveal to the user exactly what state the microcomputer is in. The status lines on an 8080 system are the same as the data lines, which when batched, provide the status of the 8080 throughout an instruction cycle. On the 8085, however, the status of the machine is provided on three lines, the S, S_0, and IO/$\overline{M}$ lines at the beginning of a machine cycle only. Besides the differences in how the signals are generated, the 8080 system generates more than one status signal per machine cycle, while the 8085 generates only one status signal per machine cycle. In other words, the 8080 outputs a memory read, an opcode fetch, and a write-out signal all at

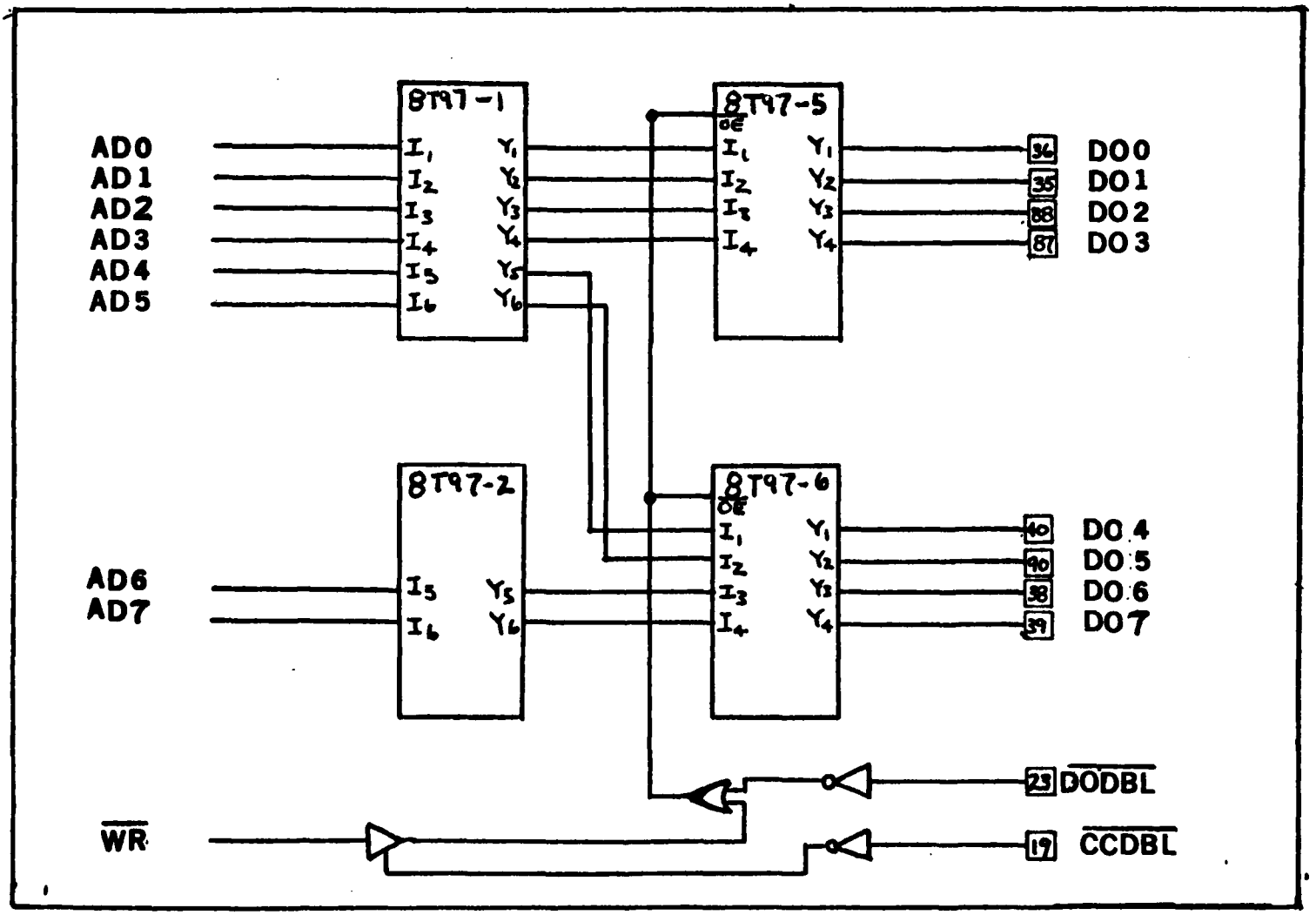


FIGURE 5. DATA OUTPUT LINES

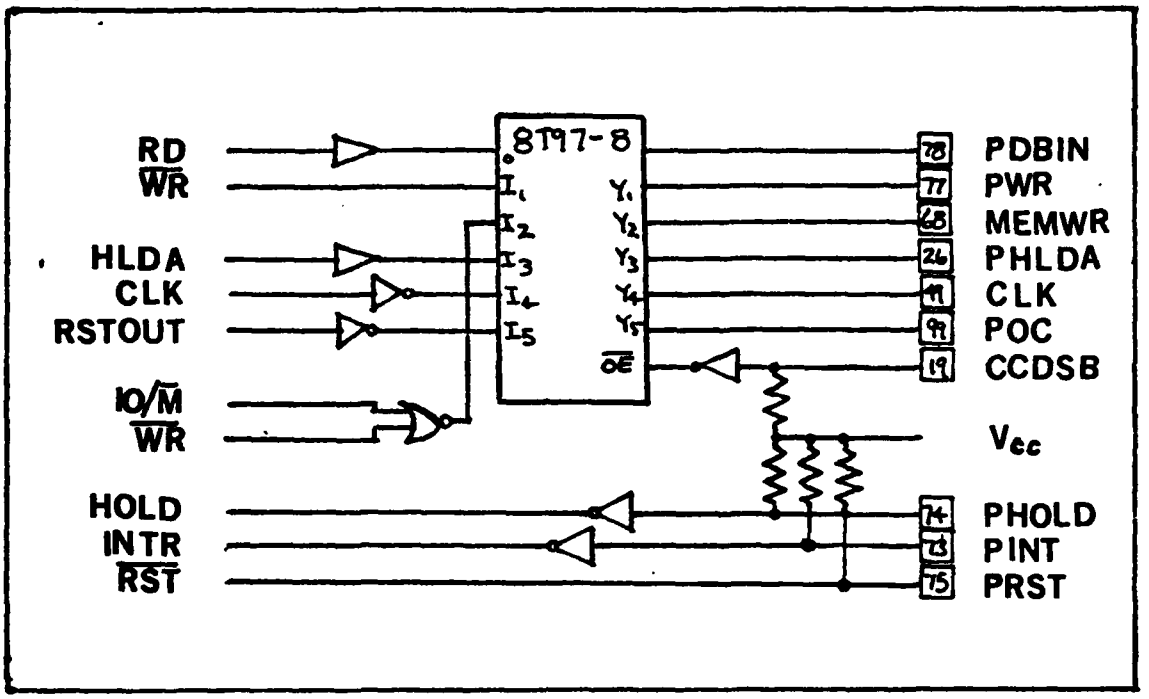


FIGURE 6. COMMAND CONTROL LINES

8080 SIGNALS	8085 SIGNALS IO/M	S1	S0
HLTA	0	0	0
MEMR	0	1	0
INP	1	1	0
WO	0	0	1
OUT	1	0	1
MI	0	1	1
INTA	1	1	1

FIGURE 7. STATUS COMPARISON

the same time for an instruction cycle. Whereas the 8085 would generate an opcode fetch for the first machine cycle, a memory read for the second machine cycle, and a write-out status for the last machine cycle. In order to make the 8085 signals compatible to the 8080 bus, many steps were involved.

First, the three bits of the 8085 status output were ordered in their eight possible binary combinations from zero to seven. Each combination was then assigned a corresponding label, identifying the state of the central processing unit for that machine cycle as shown in Figure 7. All three status bits are then fed into a high-speed three-to-eight disorder, an 8205, to generate all the status lines as they appear one at a time. Since the 8205 outputs are active low, six of the seven used decoded outputs are negated which generate the required active high signals.

At this point, the output signals of the 8205 need to be batched which provide the signals over the entire machine cycle. Looking onto Figure 8, these lines can be seen being inputted to an 8212, a high speed 8 bit latch. The 8212 has been programmed to act as a straight through buffer when the signals are valid at the beginning of each machine cycle and as a batch for the status line for the remainder of the cycle. This was accompanied by tying the mode strobe and device select number 2 lines all to five volts and inverting the Ale output to make it active low for the device select number 1 line. The active low clear line was wired to the 8085 reset out to provide all low status outputs each time the central processing unit is reset.

The last step to provide 8080 signals from the status outputs of the 8085 involved gating the batched outputs of the 8212. Three signals: MI (opcode fetch), hold acknowledge and status memory read are all necessary to produce an 8080 memory read signal. Interrupt acknowledge and MI are

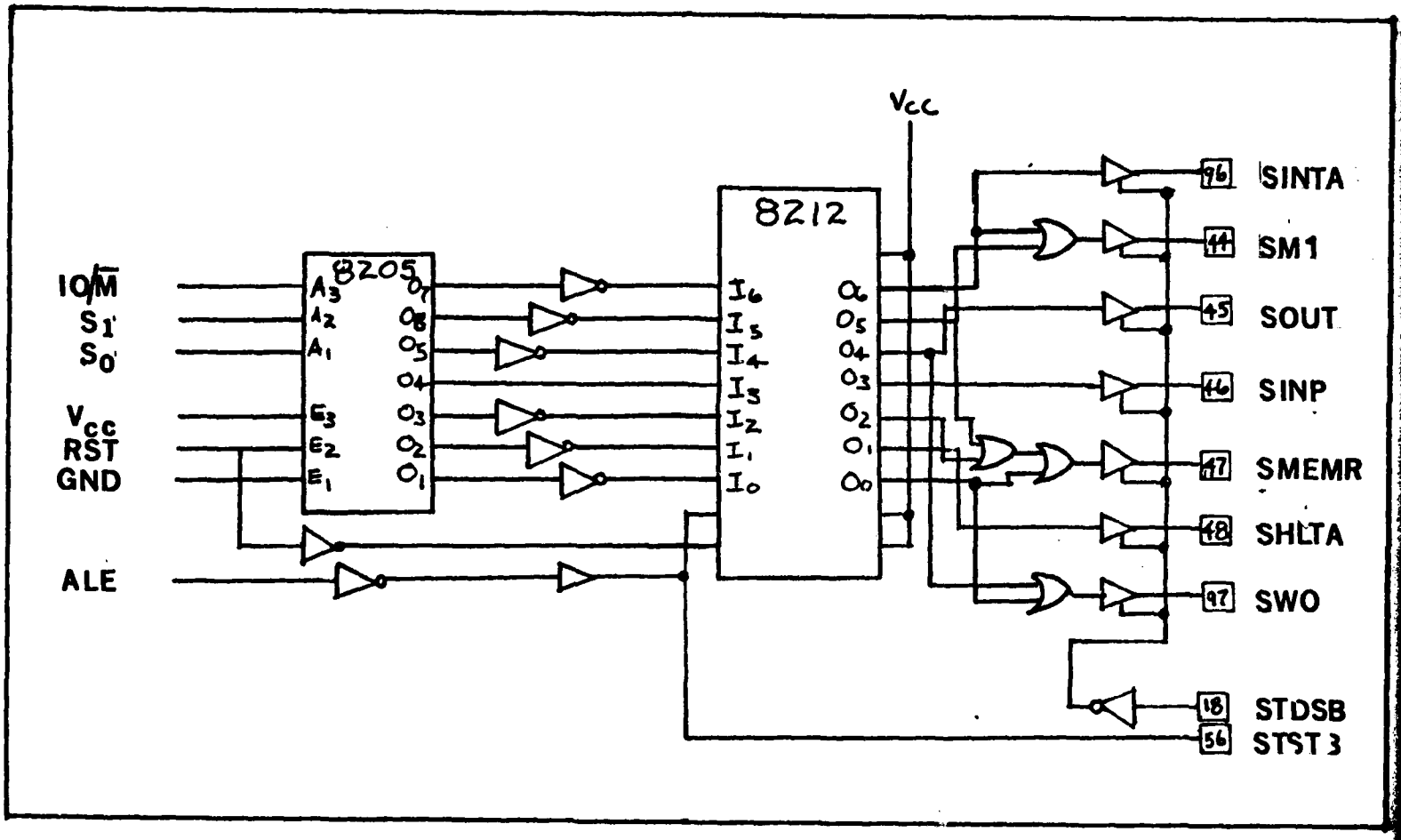


FIGURE 8. STATUS GENERATION

required to produce an 8080 MI signal, while memory write (SMWI) and I/O write (SWO) are needed to produce the status write out of the 8080. Finally, all MOW 8080 equivalent status lines are buffered through a set of 8T97's. The enable of the buffers is driven by status disable, which when active low forces the status bus into the high impedance state. The final schematic can again be seen in detail in Figure 8.

Generation of 8080 Timing Signals

In order for a computer system to run at all, timing of each device must be synchronous with the central processing unit. On the 8085, a clock output provides a clock cycle from which all peripheral devices can be run. The 8080 on the other hand, requires three very exact timing signals for the external devices. These signals are: phase one clock (Ø), phase two clock ($Ø_2$), and PSYNC.

In order to generate these signals, two 74LS123 one-shot retriggerable multivibrators were used. As shown in Figure 9a, which was derived from a combination of the 8080 and 8085 manuals, the $Ø_1$ signal is triggered from the falling edge of the clock. The $Ø_2$ signals is dependent on the falling edge of the Ø2, clock and has a pulse width of between 145 and 185 NS. Using a 74LS123 specifications table, the values for the timing resistors and the capacitors, R_T and C_{Ext}, respectively, were calculated. When added to the two multivibrators, the $Ø_1$ and $Ø_2$ signals were correctly produced. Each signal was then buffered and put on the S-100 bus as shown in Figure 9b.

The PSYNC signal is generated on the falling edge of the Ale pulse and must last at least 1 clock cycle or 333 NS for the three MH_Z clock of the 8085. Again using tables, the values for R_T and C_{Ext} were found to produce the required signal. PSYNC generation is shown in the schematic of Figure 9b.

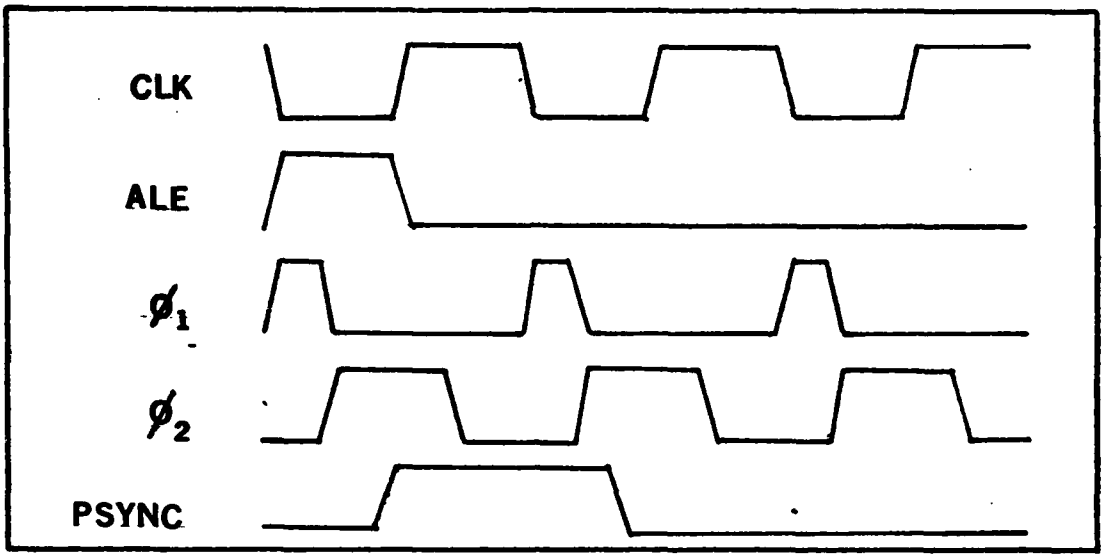


FIGURE 9a. TIMING DIAGRAM

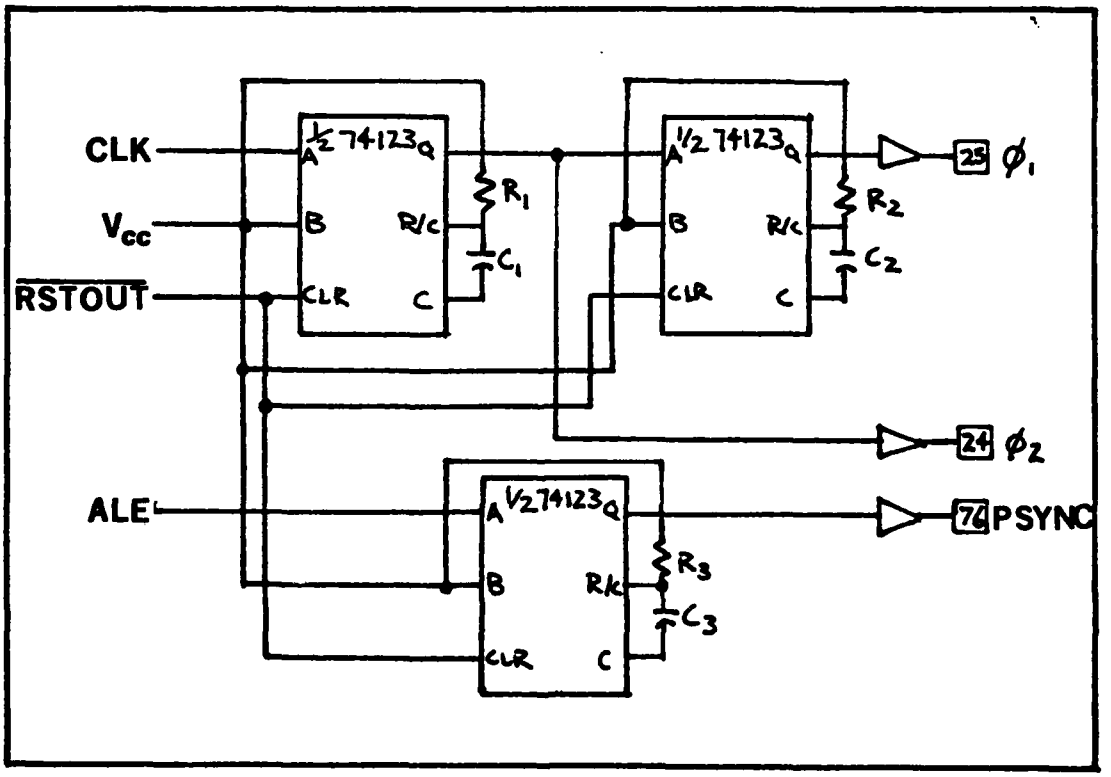


FIGURE 9b. TIMING SCHEMATIC

Pheripheral Interface

In order to interface with the pheripheral devices, input and output ports were required. By using the Intel 8156 static Ram with input/output ports, this was accomplished. The 8156 was chosen to control the pheripheral interface as it contained two eight bit parallel bi-directional ports and a command/status port. Each eight bit port was assigned a device on a dedicated basis. The A port was assigned to feed data directly to the low-speed printer,and the B port was programmed to receive the output of the input keyboard. The C port of the 8156 was programmable as either an independant six bit port or as a command/control port for the input and output ports A and B. In this the scope of this project, port C was programmed as an overseer to the operation of the A and B ports. All handshaking between the microprocessor and the pheripherals was co-ordinated through the C port by either strobing it to issue the proper commands to the pheripherals or reading its status to determine if data transfer was ready to take place. The chip enable of the 8156 is driven by a decoded address bus via an 8205. The 8205 decodes the address so that the the C port is designated as port 88, the A port is designated as port 89, and the B port is designated as port 8A, as shown in Figure 10.

One other modification was necessary in order to make the output of the microprocessor compatible to pheripherals, and this was installation of a single wait cycle in each machine cycle. By inserting a wait state in each machine cycle as shown by the schematic of Figure 11, the microprocessor was slowed sufficiently.

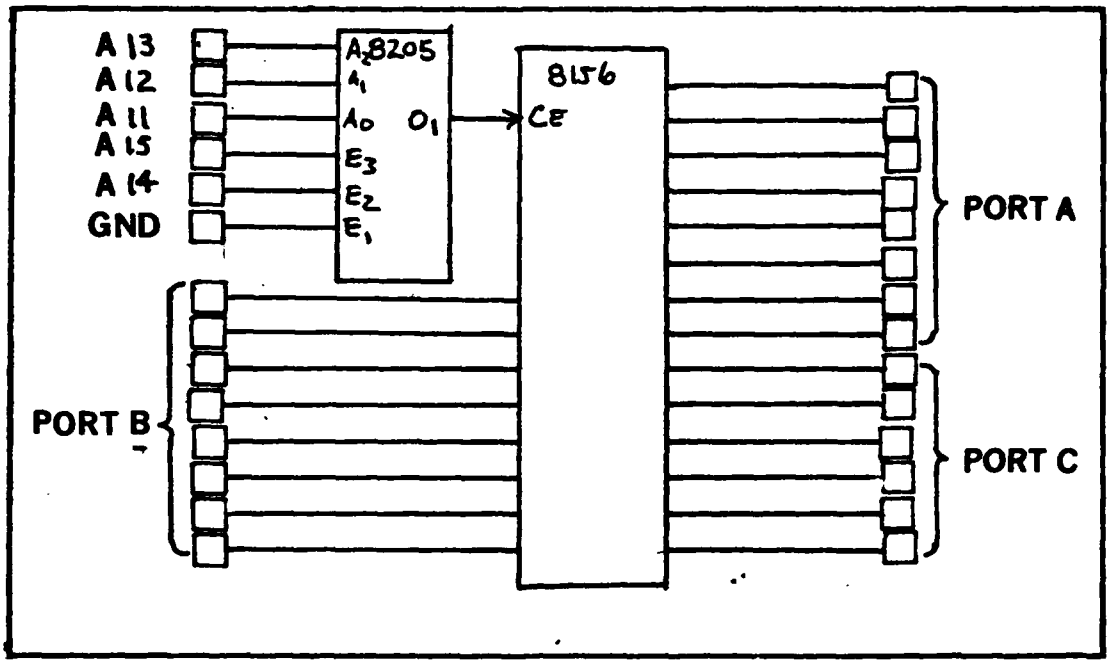


FIGURE 10. PORT DESIGNATION

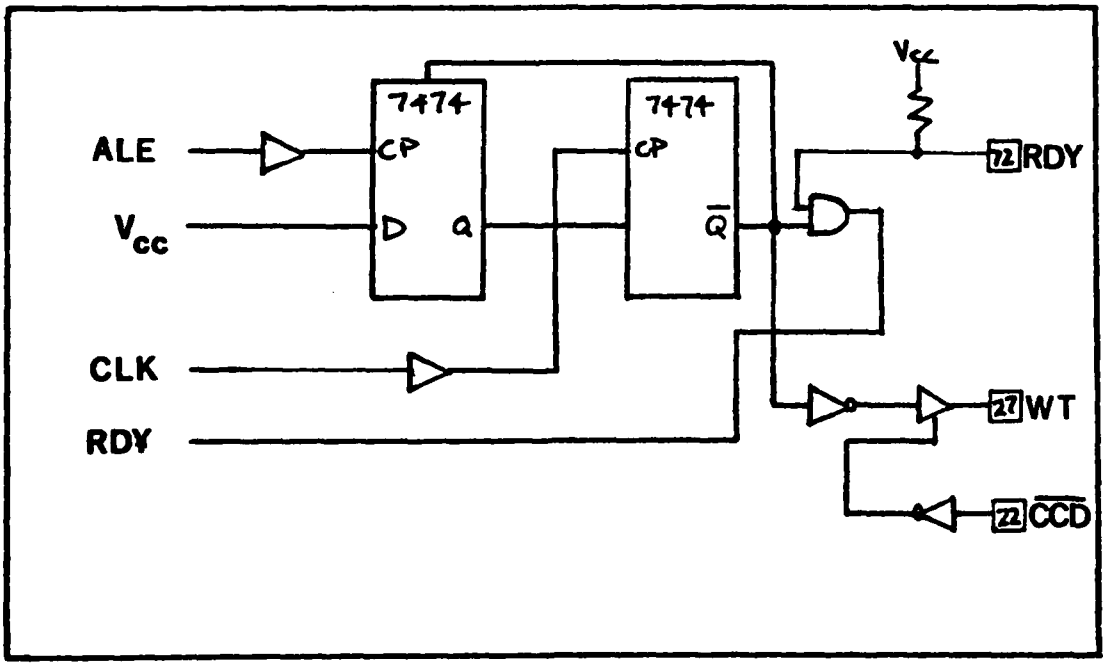


FIGURE 11. WAIT GENERATION

Power - On Jump Design

The power on jump design was adapted from the design of Z80 microprocessor power on jump design. In essence, the power on jump forces the processor to make an immediate jump to a preset address. This causes the processor to start executing programs at location E8ØØ hex which is the starting location of the disk controller as opposed to execution starting at ØØØØ as the processor would normally do.

To do this jump requires a C3 ØØ E8 three byte command (C3 is JMP immediate in 8085 software), to be fed into the data lines of the microprocessor in three consecutive clock pulses, immediately after power up or upon a reset command. The circuit of Figure 12 is a working example of how this is done.

As soon as a power-on or reset occurs, the reset out pin of the 8085 goes high, clearing the 74LS175 through the master reset pin.

At this point all Q outputs of the LS175 are set low, and the $\overline{Q}$ outputs are high until the next clock pulse occurs. These clock pulses are supplied by the output of the nand gate. The nand gating of $\overline{RD}$ and $\overline{POJ\text{-}DONE}$ yields a zero when both are high and zero at all other times. Therefore, for each of the first three clock cycles, as $\overline{RD}$ goes low and is gated with $\overline{PJ\text{-}DONE}$, the output of the nand gat drops to zero and then high again. The LS175 is rising edge triggered, so at this point each of the four D flip-flops is loaded. From the configuration of Figure 11 it can be seen that a "1" is loaded into FF#1, and all others load zeros.

A stream of "1"'s are circulated through the flip flops until the third clock pulse (MX-EN) occurs. At the end of the third pulse, the status of $\overline{PJ\text{-}DONE}$ is high, and obviously $\overline{POJ\text{-}DONE}$ is zero. Now that $\overline{POJ\text{-}DONE}$ is zero,

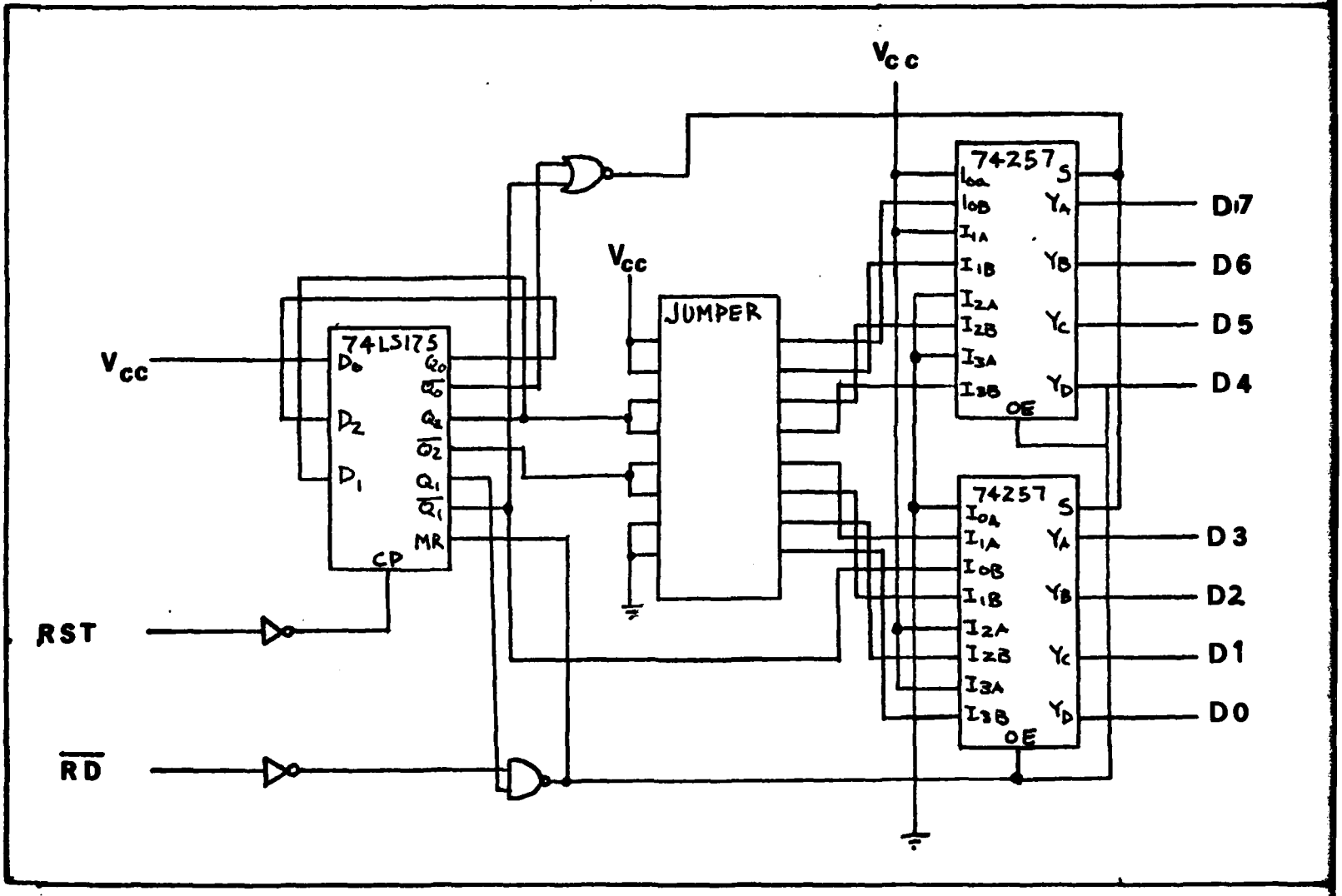


FIGURE 12a. POWER-ON JUMP

the nand output (MX-EN) will always be high, as the MX-EN output remains high for the $\overline{\text{POJ-DONE}}$ equals with zero regardless of the state of RD. This in turn shuts down the LS175 as no more rising edges will be available with the clock input, unless another reset is hit.

The rest of the circuit is also active during this period. The 16 pin jumper socket helps to decode the POJQZ and POJDONE signals which provide the correct jumped to address. This address is fed into the multiplexers and after careful selection, it is fed into the 8085.

Selection of output is done by the POJS (power on jump select) line of Figure 12. When the POJQ1 and POJQ2 lines are zeros as they are at the end of clock pulse 3, the POJS is high, and the I inputs are selected to be outputted. During the first two clock cycles, one or both of POJQ1 and POJQ2 are high, therefore, forcing POJS to be low. POJS then allows only the I_0 inputs to be outputted during the first two clock cycles. This is the point where the C3 and ØØ are forced onto the data bus. When I_1 is high in t last clock pulse, E8 is loaded onto the data bus, thereby forcing the processor to jump to location E800 for execution of the disk controller.

Initialization of System and System Start Up

In order to bring the system up and running, the next step was to create a working floppy disk to initialize the system. Software programming in 8080 compatible assembly language was required to set-up the disk. These consisted of four routines, one each for input of a character, output of a character, control C command, and the initialization of the mother board.

In order to input a character, the C port of the 8156 is sampled until pin C_5 goes high. If L_5 is high then a character has been typed in the

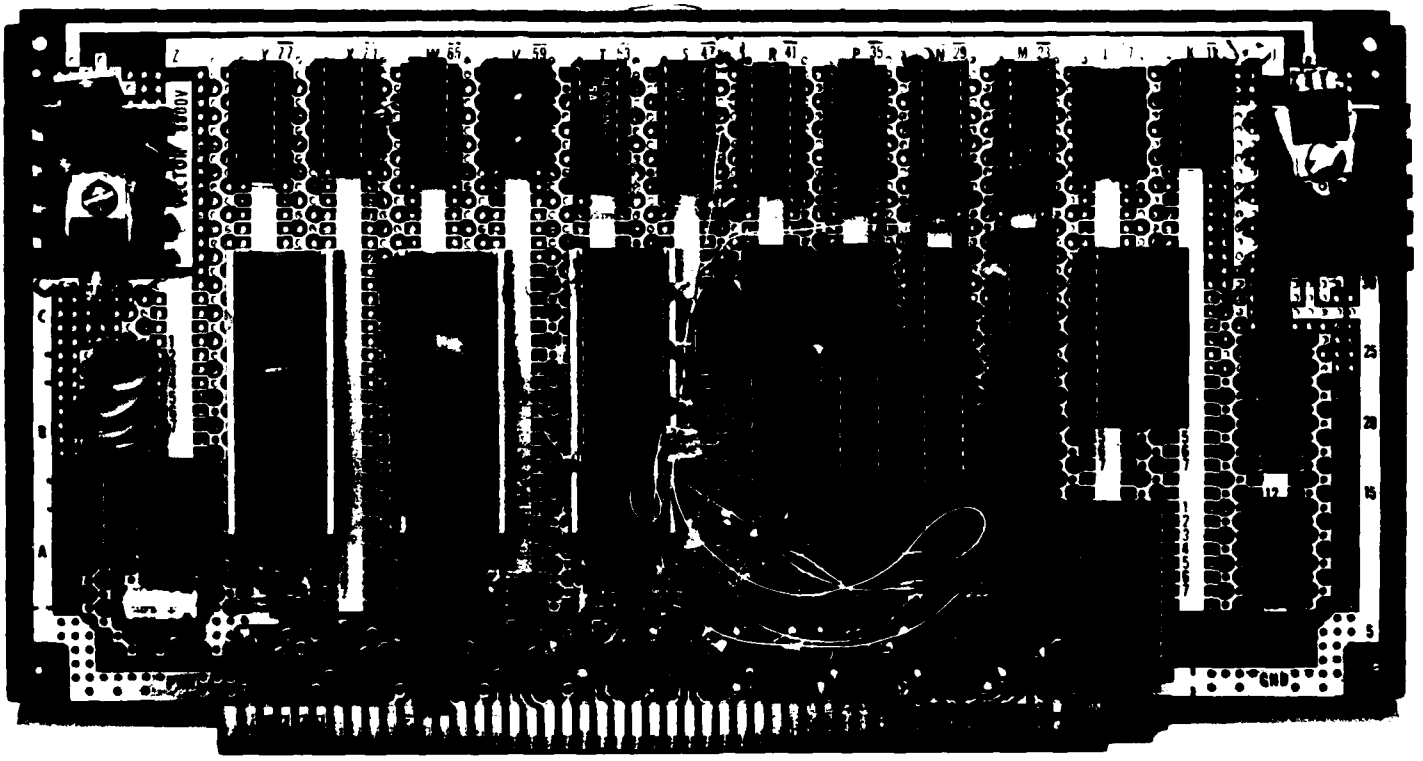


FIGURE 12b. COMPUTER: COMPONENT SIDE

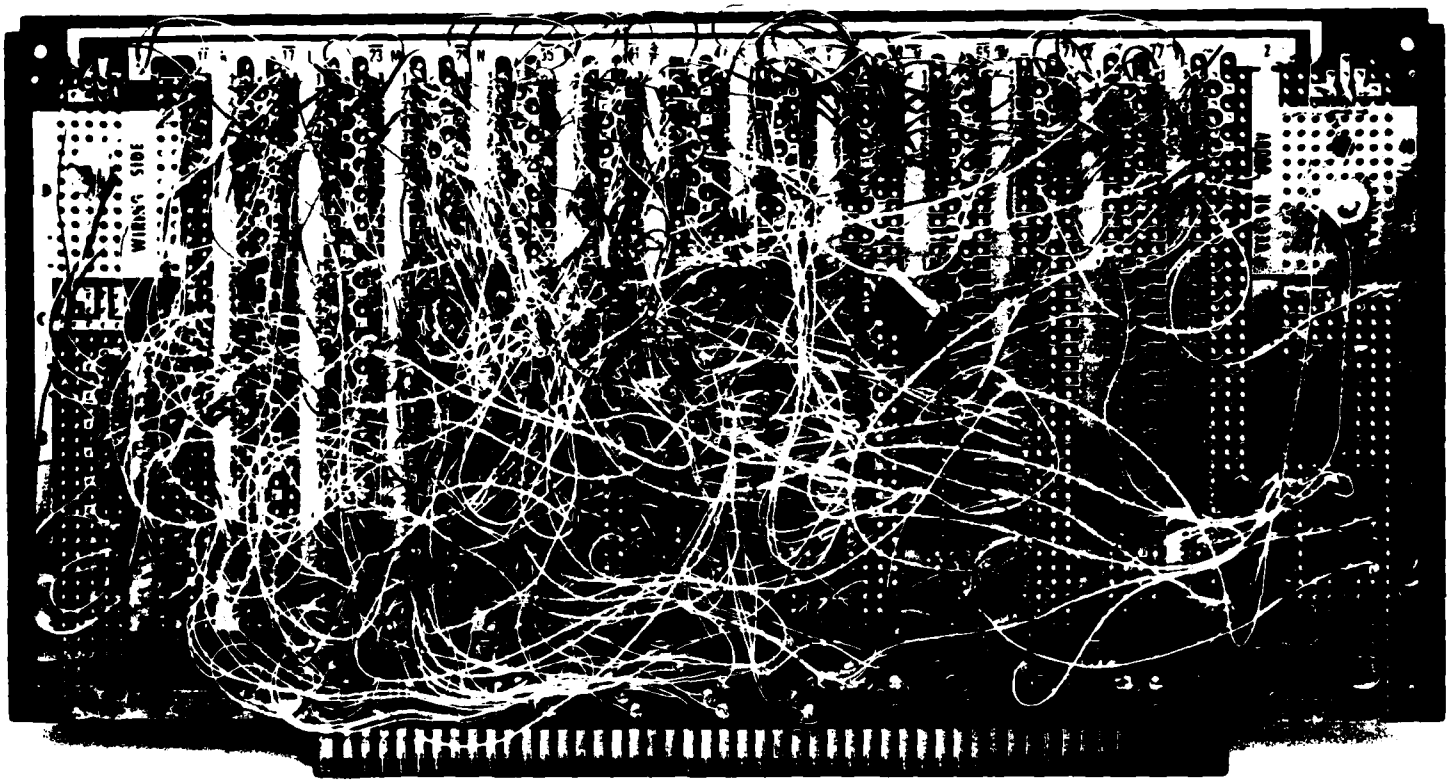


FIGURE 12c. COMPUTER: WIRING SIDE

keyboard. The character is then inputted through the 8156 "A" port and demasked to remove the key struck bit. The program then returns to the running program and stops.

In order to output a character, the C port of the 8156 is sampled to see if the printer is ready. If ready, the character is outputed through the B port of the 8156. The character is then removed from the B register and loaded into the accumulater as required by the DOS before return. After returning to the main program, the output character program COU7 is completed.

The next program to be completed is the control C input routine (CONTC). In essence, if a control C has been typed, then the routine sets the processor zero flag. If no character was typed or the character was not a control C, the zero flag is then cleared. In either event, as soon as the zero flag is set to its proper value, the CONTC routine returns to the main program.

The last routine needed was the initialization routine, TINIT. This routine was used to initialize the output parts of the 8156 to provide one input port. This particular set up was chosen to allow the most system flexibility. Upon completion of the routine, a return to the main program was done as shown in Figure 12.

Figure 13 shows the assembled program. After assembly, the start of each individual was loaded into a jump table in the DOS. Therefore, as each routine was needed, it was then jumped to. This modified jump table is shown in Figure 14.

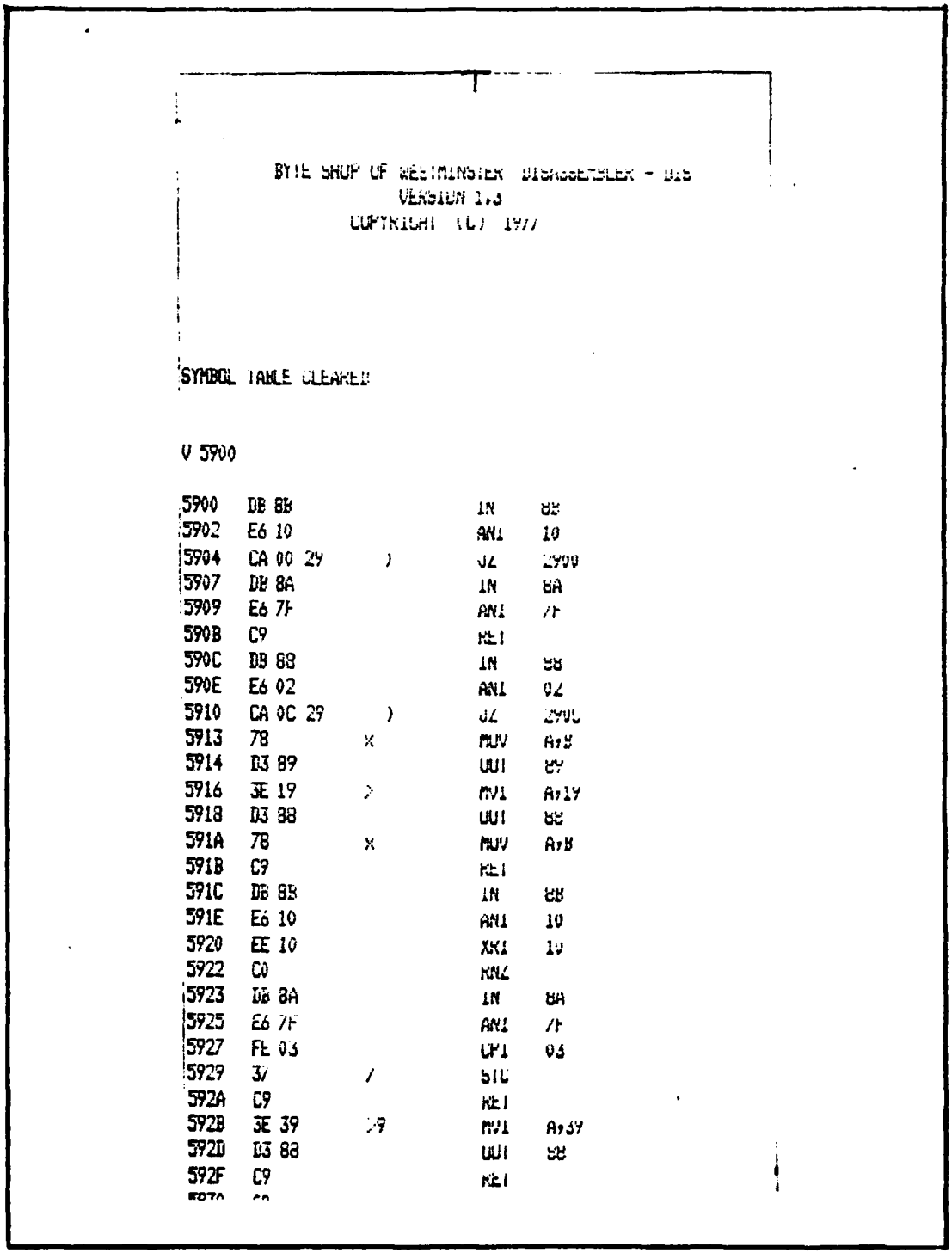


FIGURE 13. INPUT ROUTINES

```
                BYTE SHOP OF WESTMINSTER  DISASSEMBLER - DIS
                        VERSION 1.5
                        COPYRIGHT (C) 1977



SYMBOL TABLE CLEARED


V 200D

200D   C3 0C 29      )        JMP    290C
2010   C3 00 29      )        JMP    2900
2013   C3 2B 29      +)       JMP    292B
2016   C3 1C 29      )        JMP    291C
```

FIGURE 14. ROUTINE JUMP TABLE

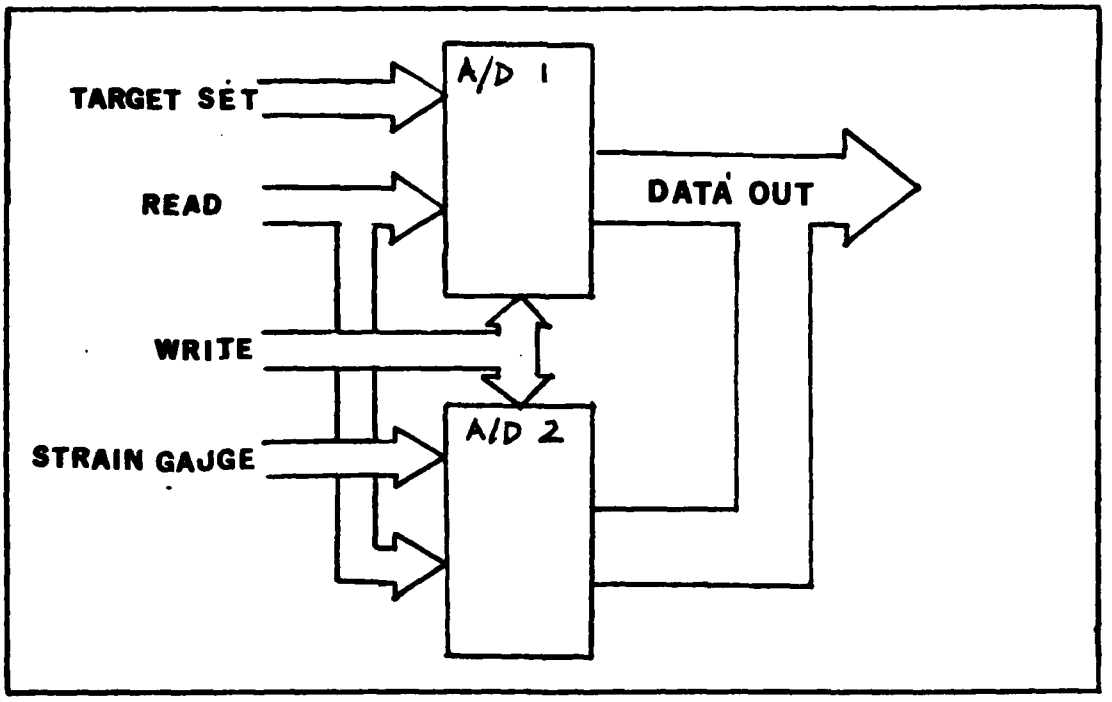


FIGURE 15. A/D BLOCK DIAGRAM

III. Test Apparatus

Once the 8085 computer system was constructed and tested, the remainder of the stimulation apparatus was to be built. This consisted of three parts: design and contruction of the feedback analog to digital channels, design and construction of the digital to analog controlled stimulators and production of the assembly language programming to control the stimulation. Both pieces of hardware, the feedback channels and the stimulators, occupied the same S-100 mother board in order to conserve space and material. The software was done in assembly language to provide the quickest response to changes in feedback information.

Design and Construction of Feedback Channels

In order to insure an isometric contraction was maintained from initial contraction through muscle fatigue, two channels of digitized information are needed. These channels relay the digital outputs of the target tension and the feedback loop of the strain gauge as blocked out in Figure 15. The target tension is adjusted at the onset of experimentation and remains a constant, however, the output of the strain gauge is a variable and is continuously sampled. Both analog inputs are fed into analog to digital converters mapped into memory space. When either port is selected by the 8085, the value of its respective analog input is strobed onto the S-100 data bus. At this point the 8085 interprets the input and outputs a corresponding correction factor to the output channels.

Figure 15 details the two channels of analog to digital information. Both A/D 0804 chips are memory mapped. The input address lines are decoded by the 8205 decoder such that if the address bus contains a location between

9000 and 9799H the target set A/D (A/D #2) is selected, if the location is between 9800 H and 9FFF H the strain gauge feedback A/D (A/D #2) is selected. The chip select for each of the AD 0804 chips is active low, allowing for direct compatibility with the active low outputs of the 8205. When the write input ($\overline{WR}$) is driven low in conjunction with a low signal on the chip select, the selected chip will reset itself. As the write lines go high at the end of the pulse, conversion of the analog input begins. The results of the conversion are then mapped into an internal eight, bit, tri-state output batch. Until enabled, the output of the 8 bit latch and of the A/D chip is a high impedance state.

The output latches are enabled only when both the chip select, and the read line are driven low. The N.S. chip enable and the read input are the inputs to an internal nor gate. The output of the gate drives the active high enable of the internal latch. When the latch is enabled, the output of the analog to digital converter changes from tri-state to valid data. The data remains valid for 125 us and drives the data lines of the S-100 bus through two 8T97 driven chips. At the end of the valid data time, the output of each A/D transitions to the high impedance state.

An interrupt output is generated by each ADC0804 when conversion is started, and it functions as a flag for the 8085. The interrupt output ($\overline{PINT}$) is active low and is driven low when each conversion begins. If the A/D chip is read, then the interrupt output returns high. If not, the pin remains low until the conversion is again requested. By gating the two interrupt outputs through a NOR gate, the data out of the converters is available to the S-100 bus between each conversion request.

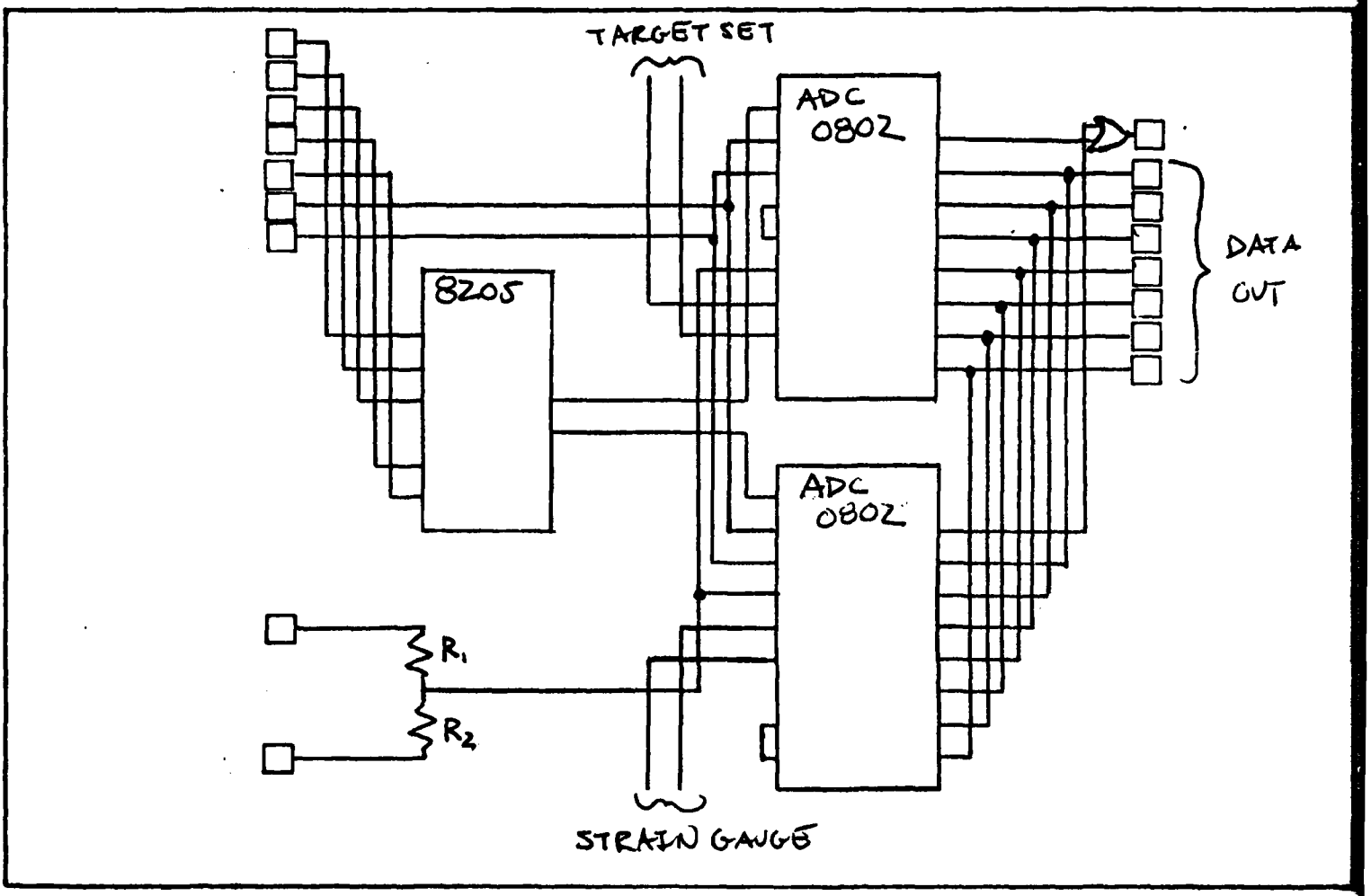


FIGURE 16. A/D FEEDBACK CHANNELS

Each ADC0804 must be driven by a clock. Since the maximum speed of the converter is substantially slower than the 8085 clock, a clock was made from an RC circuit to drive the clock inputs (not shown) at a frequency of 606 KH. At this clock speed, conversion time was 100 NS.

After the two channels of converters were constructed, they were tested for accuracy and then placed into the computer. The analog inputs were then attached to the target voltage and the strain gauge bridge and the feedback look was ready for operation.

Design and Construction of Stimulators

In order to construct the nerve stimulators, research was done and a model was found. Adaptations of the model produced the block diagram for the stimulators as shown in Figure 17. Each digital to analog converter has been placed in memory as an I/O port. The 8085 transmits signals to each port for adjustments in the stimulation. The first converter controls the rate at which the voltage controlled oscillator operates. The oscillator output is fed into a binary-coded decimal (BCD) counter which in turn drives a BCD to decimal decoder. Outputs zero through two of the decoder produces the three sequential pulses needed as a minimum for smooth muscle contraction.

Amplitude of the pulses is controlled by the second digital to analog converter. Converter output drives the non-inverting input of the amplifiers controlling the pulse amplitude. The last computer controller digital to analog channel controls the voltage of the anodal blocking electrodes. Manipulation of these electrodes, results in blocking the three pulses from the stimulating electrodes so as to induce an orderly recruitment of motor units.

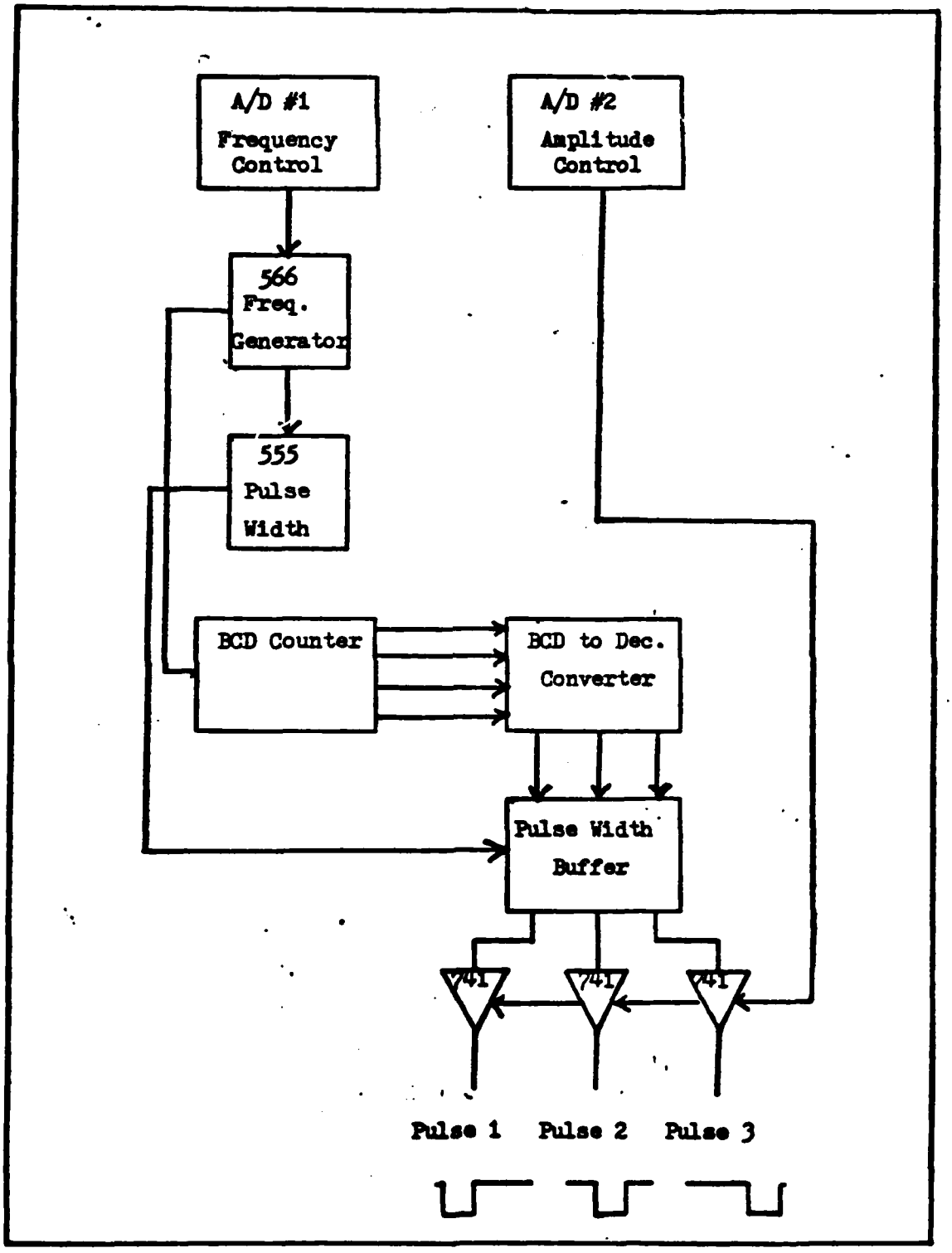


FIGURE 17. D/A CONTROLLED STIMULATORS BLOCK DIAGRAM

Figure 18 outlines the implementation of the digital to analog converters. Converters were chosen to be microprocessor compatible for the minimum amount of additional circuity and buffering. Each converter is selected after decoding the A_{11} - A_{15} address lines though an 8205 high speed, one out of eight. Individual chip selects are active low as are the outputs of the decoder, thus no gating is necessary. Required to be at least 250 ns in width by the converters, the write output of the 8085 is 500 ns in length and therefore just qualifies as valid input to the digital to analog converter. Thus, the DAL0832 eight-bit digital to analog converters are directly compatible for the 8085 system.

Figure 18 illustrates how each converter is set up. All share common data bus lines and input write lines. When a single converter is selected for output, both the $\overline{CS}$ and the write line must be low. This causes the information on the data bus to be inputted to the internal eight-bit register. Next, the transfer line output of the 8205 decoder in conjunction with a low input on the write line number 2 causes the data to be outputted to the operational amplifier. Since this output signal is in the form of two output currents, the amplifiers are necessary to transform these into voltages. The output of two of the converter amplifiers are used in turn to drive the stimulators. The last converter amplifier drives a second amplifier and is the anodal block buffer.

Figure 19 details the schematic of the stimulator circuit. The output of the first digital to analog converter is fed into the control voltage of the LM566 voltage controlled oscillator. As the output of the converter amplifier varies from two to five volts, the frequency output of the oscillator changes from zero to two times the normalized frequency. The

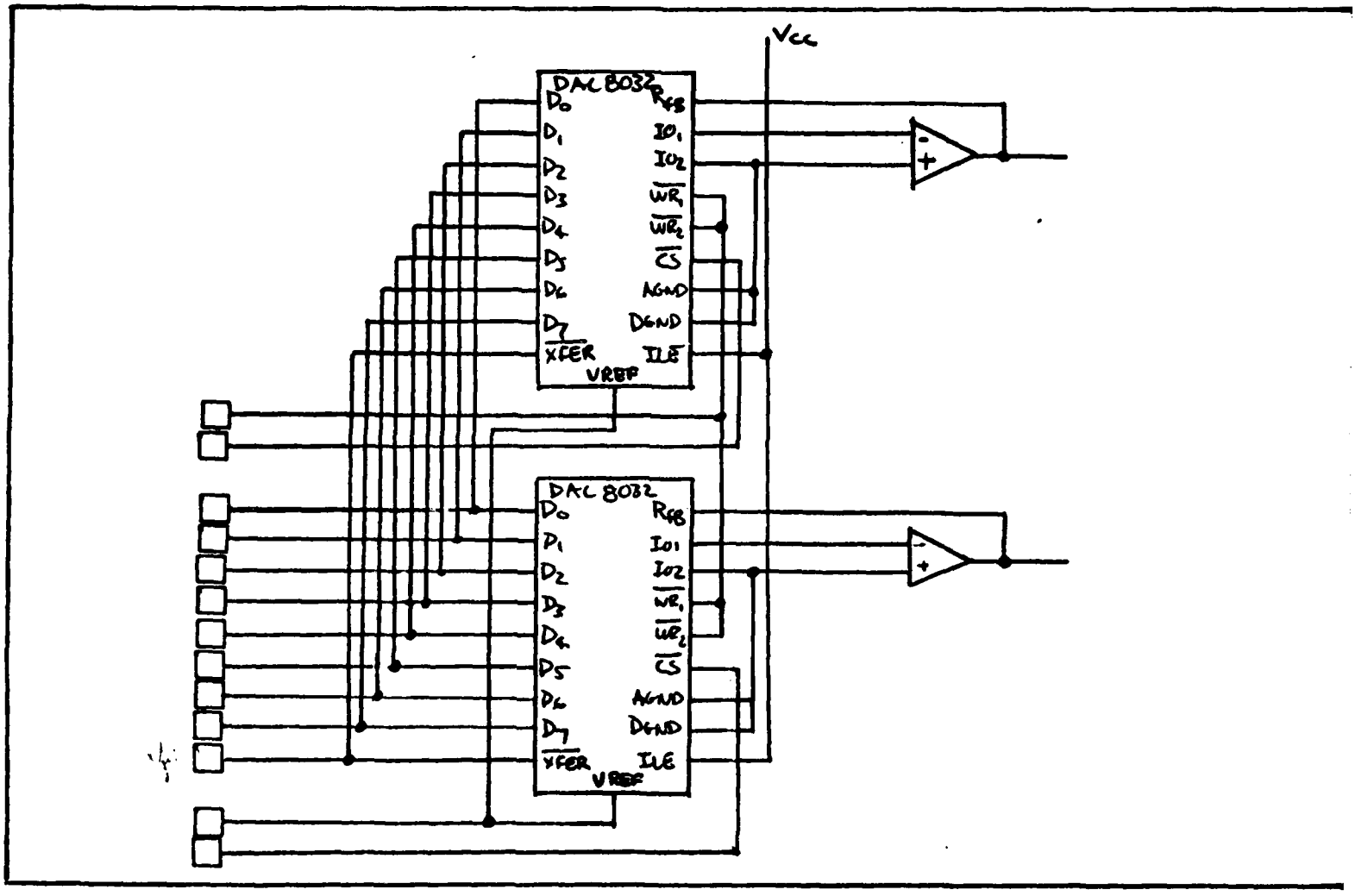


FIGURE 18. D/A CHANNELS

normalized frequency was set at approximately 50 H_z by using timing resistors and capacitors of values four KΩ and 1μF, respectively. Therefore, by varying the analog output of the converters, the frequency of stimulation ranges from 0 to 100 Hz.

The output of the voltage controlled oscillator drives the input of the 7490 binary-coded decimal counter. The counter has been set up with pins six and seven grounded and pins two and three set to the output of the OR gate, so as to provide reset to zero at the beginning of each fourth count. Outputs of the BCD counter are directed into the inputs of the 7442 BCD-to-decimal decoder.

Each time the count of the BCD counter changes in its transition from zero to ten, one decoder output (active low) is activated. By this means, three sequential pulses are generated as the counter moves from zero to two. On the fourth count the output of the decoder is inverted to active high, and the 7490 counter is cleared to start at zero once again. By this method as many as nine sequential stimulator pulses may be generated, the counter beginning at zero after being cleared by the tenth count. However, for simplicity only three pulses were used in this project.

Each sequential pulse from the decoder is first inverted for use as a stimulator pulse. Now the individual pulses are fed into channels of an 8797 buffer. The buffer is enabled by the output of the LM555 pulse width control timer. For each clock pulse of the LM566 oscillator, the trigger of the LM555 is activated, and a control pulse from the LM555 is released. The width of the control pulse was set at 100 μs by use of a 0.01 μF timing capacitor and a 10 KΩ timing resistor. Each control pulse arriving in conjunction with the stimulator pulse at the buffer created a controlled

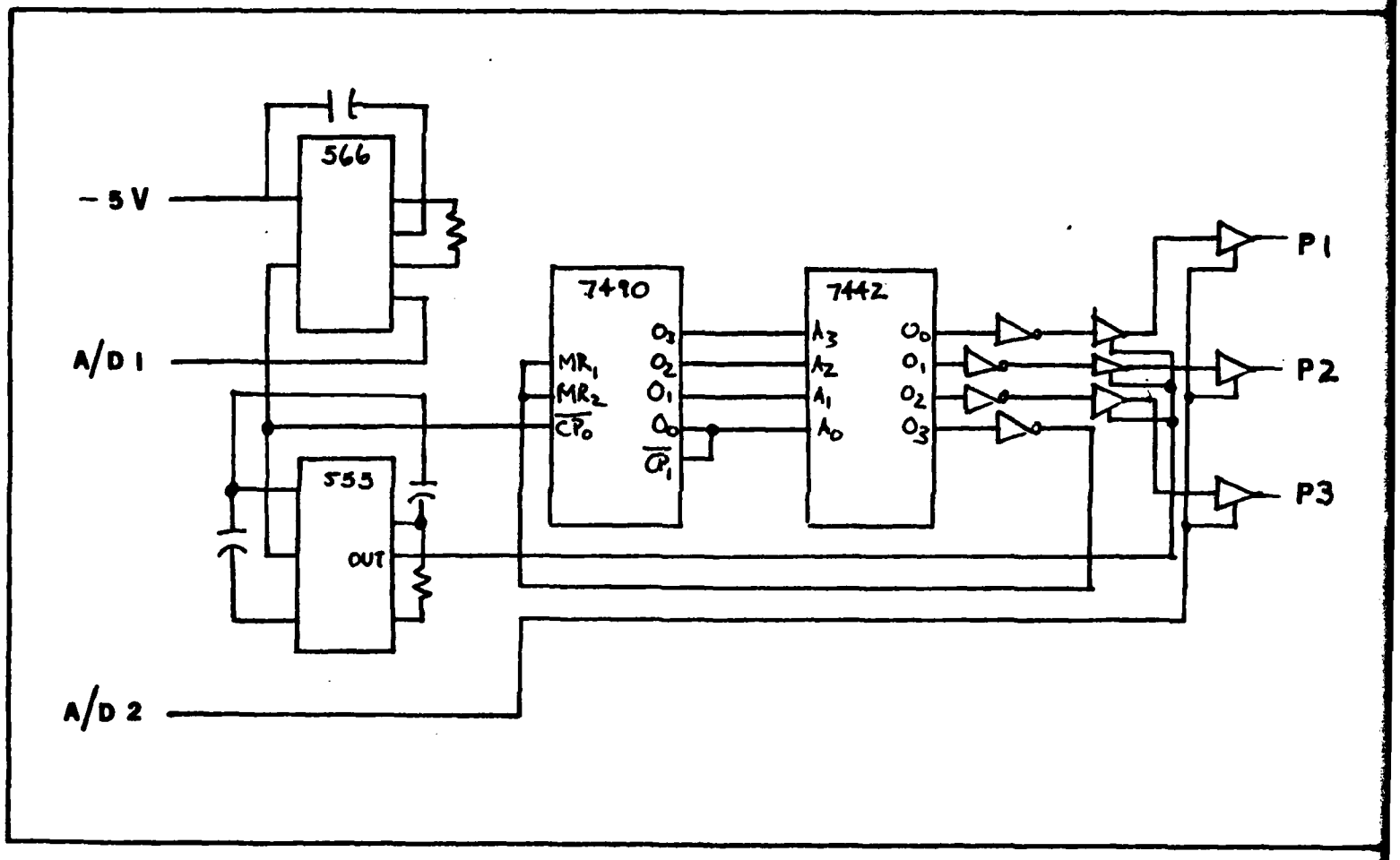


FIGURE 19. STIMULATOR SCHEMATIC

width stimulation pulse of less than 100 μS. When the input to the individual buffer is not selected or the enable is high, the output of the buffer is tri-stated. By tying each buffer output to ground, the input to the amplitude control amplifiers is zero when the pulse is not selected.

Each stimulator pulse, now width controlled, is inputted to the inverting input of an operational amplifier. The operational amplifier has been designed such that the gain of the amplifier is three, and the relative value of the output voltage is controlled by the second digital to analog converter. This allows for voltage swings of 0 to 15 volts, ranging from a baseline set by the output of the digital to analog converter from 0 to +5 volts.

Stimulation Programming

To control the stimulation a controlling program is required to ensure accurate stimulation occurs. All the stimulation programming was done in 8080 assembly language and stored on disk memory. By using assembly language programming, quick response to tension changes are made.

The block diagram of figure 20, gives an overview of the stimulation programming. First, the entire system is initialized in preparation for the stimulation. Next, the first sequence of stimulation pulses is released at a frequency of 10 Hz. After the pulses are released and the muscle starts to contact, the feedback from the strain gauge bridge is sampled at a rate of ten times per second. The output of the strain gauge bridge is then directly compared to the digitized input of the manually set target tension digital-to-analog converter.

If a difference of $\pm$ 2% is noted between the two inputs, the computer's program adjusts the output amplitude of the stimulation pulse from the

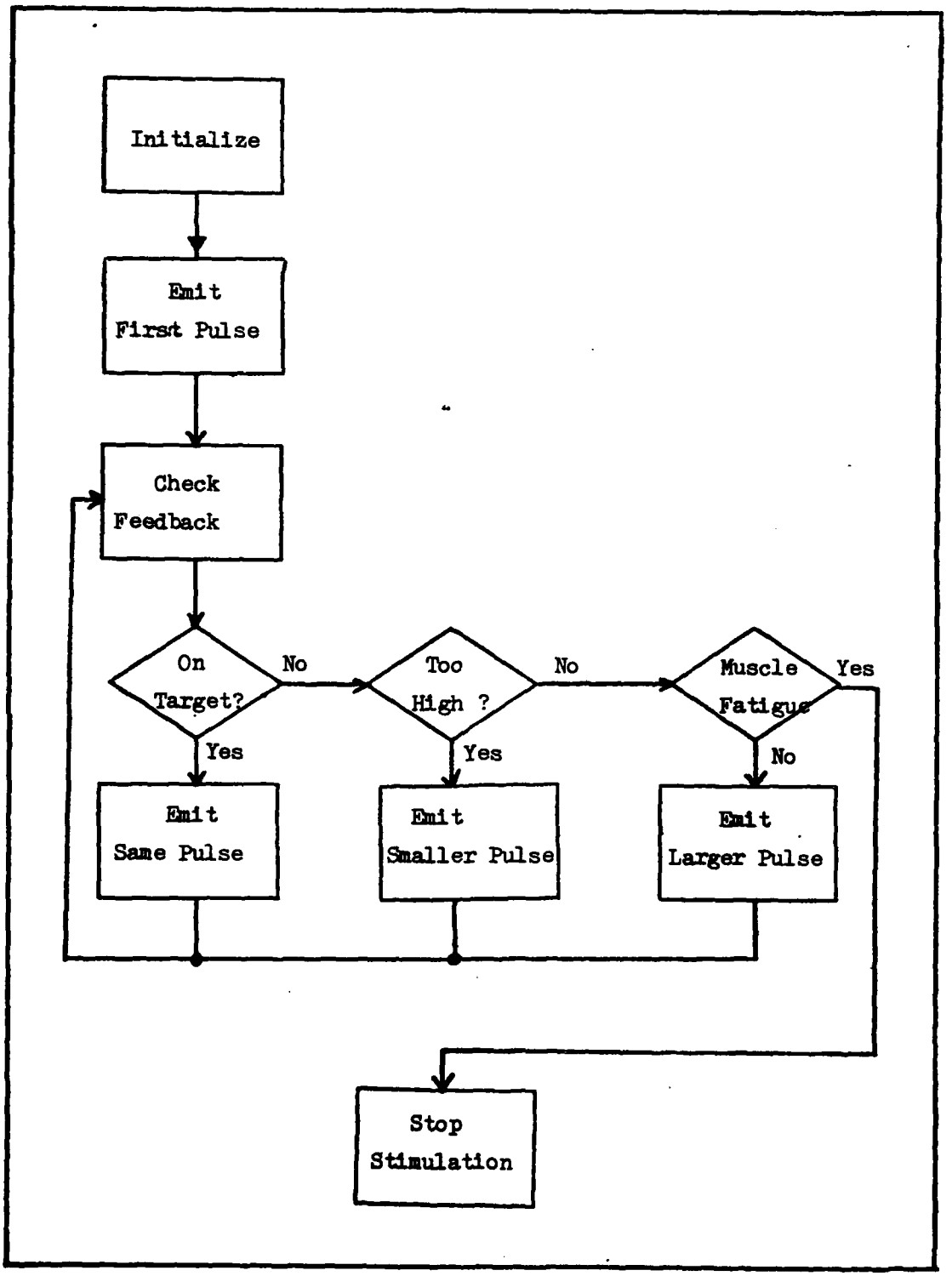
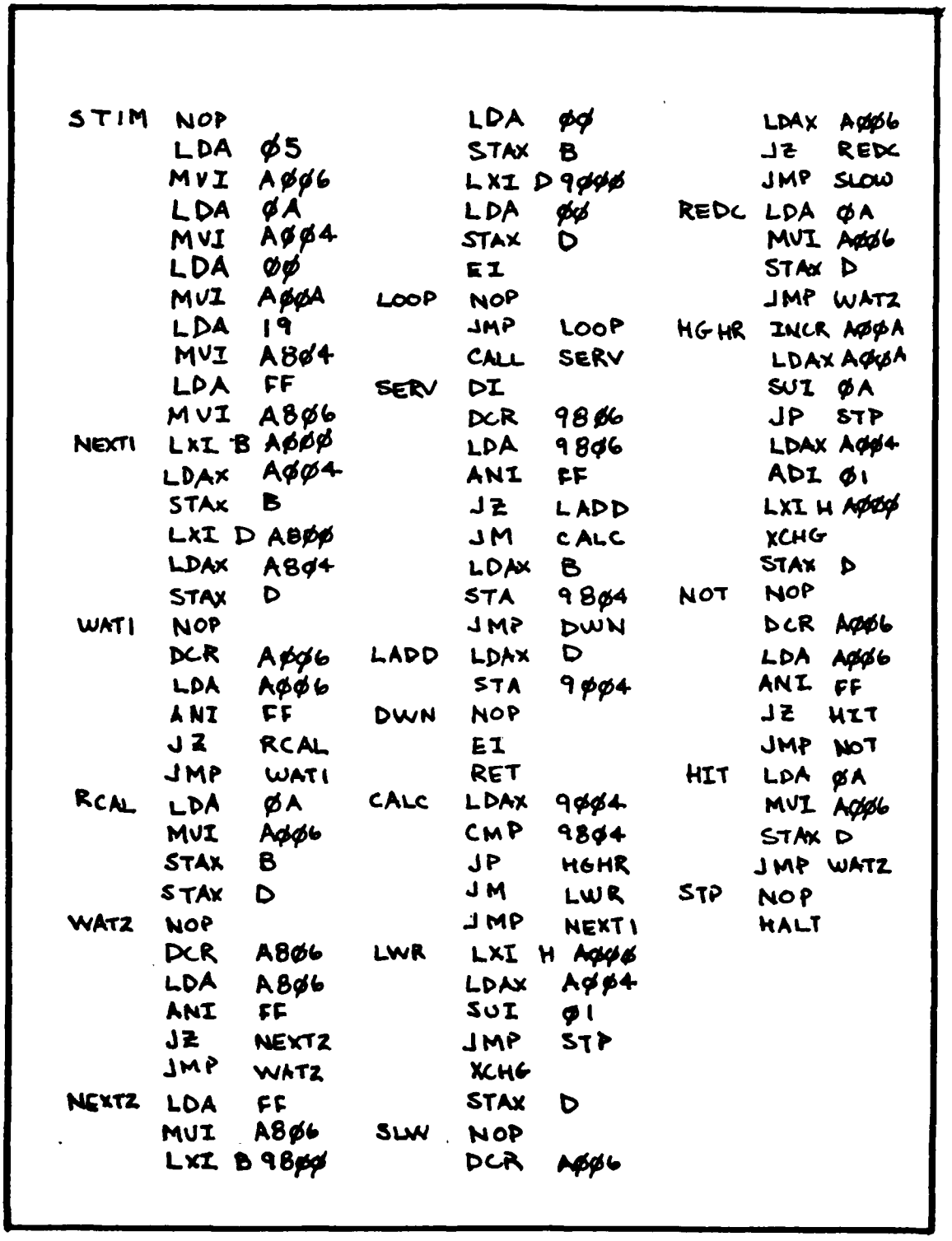


FIGURE 20. STIMULATION BLOCK PROGRAMMING

initial setting of 0.25 volts. The adjustment factor was calculated to increase or decrease theoutput amplitude of the pulses by a factor of 0.05 volts per 2.0% discrepancy. As the muscle tired and recruitment of all motor units was accomplished, the target tension was increasingly more difficult for the computer to maintain. At this point, if the error between the target tension and actual muscle tension exceeded 10% for more than three consecutive pulses, the computer terminated the stimulation and the muscle was deemed fatigued.

An assembled copy of the actual software program is shown in Figure 21. Comments are made on the margin to explain each block of programming.



```
STIM  NOP
      LDA  Ø5
      MVI  AØØ6
      LDA  ØA
      MVI  AØØ4
      LDA  ØØ
      MVI  AØØA
      LDA  19
      MVI  A8Ø4
      LDA  FF
      MVI  A8Ø6
NEXTI LXI B AØØØ
      LDAX AØØ4
      STAX B
      LXI D A8ØØ
      LDAX A8Ø4
      STAX D
WATI  NOP
      DCR  AØØ6
      LDA  AØØ6
      ANI  FF
      JZ   RCAL
      JMP  WATI
RCAL  LDA  ØA
      MVI  AØØ6
      STAX B
      STAX D
WATZ  NOP
      DCR  A8Ø6
      LDA  A8Ø6
      ANI  FF
      JZ   NEXTZ
      JMP  WATZ
NEXTZ LDA  FF
      MVI  A8Ø6
      LXI B 98ØØ
      LDA  ØØ
      STAX B
      LXI D 9ØØØ
      LDA  ØØ
      STAX D
      EI
LOOP  NOP
      JMP  LOOP
      CALL SERV
SERV  DI
      DCR  98Ø6
      LDA  98Ø6
      ANI  FF
      JZ   LADD
      JM   CALC
      LDAX B
      STA  98Ø4
      JMP  DWN
LADD  LDAX D
      STA  9Ø4
DWN   NOP
      EI
      RET
CALC  LDAX 9ØØ4
      CMP  98Ø4
      JP   HGHR
      JM   LWR
      JMP  NEXTI
LWR   LXI H AØØØ
      LDAX AØØ4
      SUI  Ø1
      JMP  STP
      XCHG
      STAX D
SLW   NOP
      DCR  AØØ6
      LDAX AØØ6
      JZ   REDC
      JMP  SLOW
REDC  LDA  ØA
      MVI  AØØ6
      STAX D
      JMP  WATZ
HGHR  INCR AØØA
      LDAX AØØA
      SUI  ØA
      JP   STP
      LDAX AØØ4
      ADI  Ø1
      LXI H AØØØ
      XCHG
      STAX D
NOT   NOP
      DCR  AØØ6
      LDA  AØØ6
      ANI  FF
      JZ   HIT
      JMP  NOT
HIT   LDA  ØA
      MVI  AØØ6
      STAX D
      JMP  WATZ
STP   NOP
      HALT
```

FIGURE 21. STIMULATION PROGRAMMING

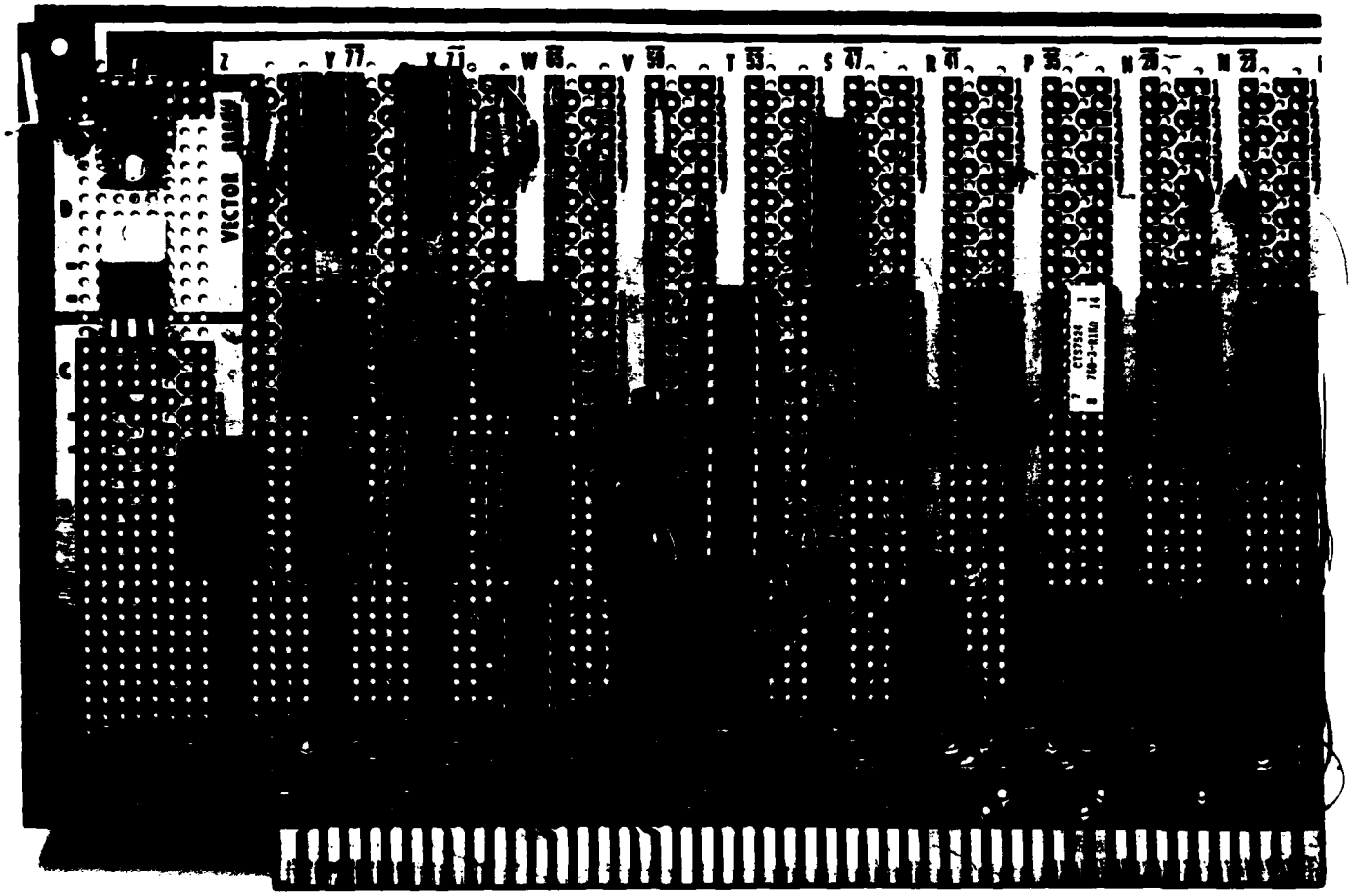


FIGURE 22. STIMULATORS: COMPONENT SIDE

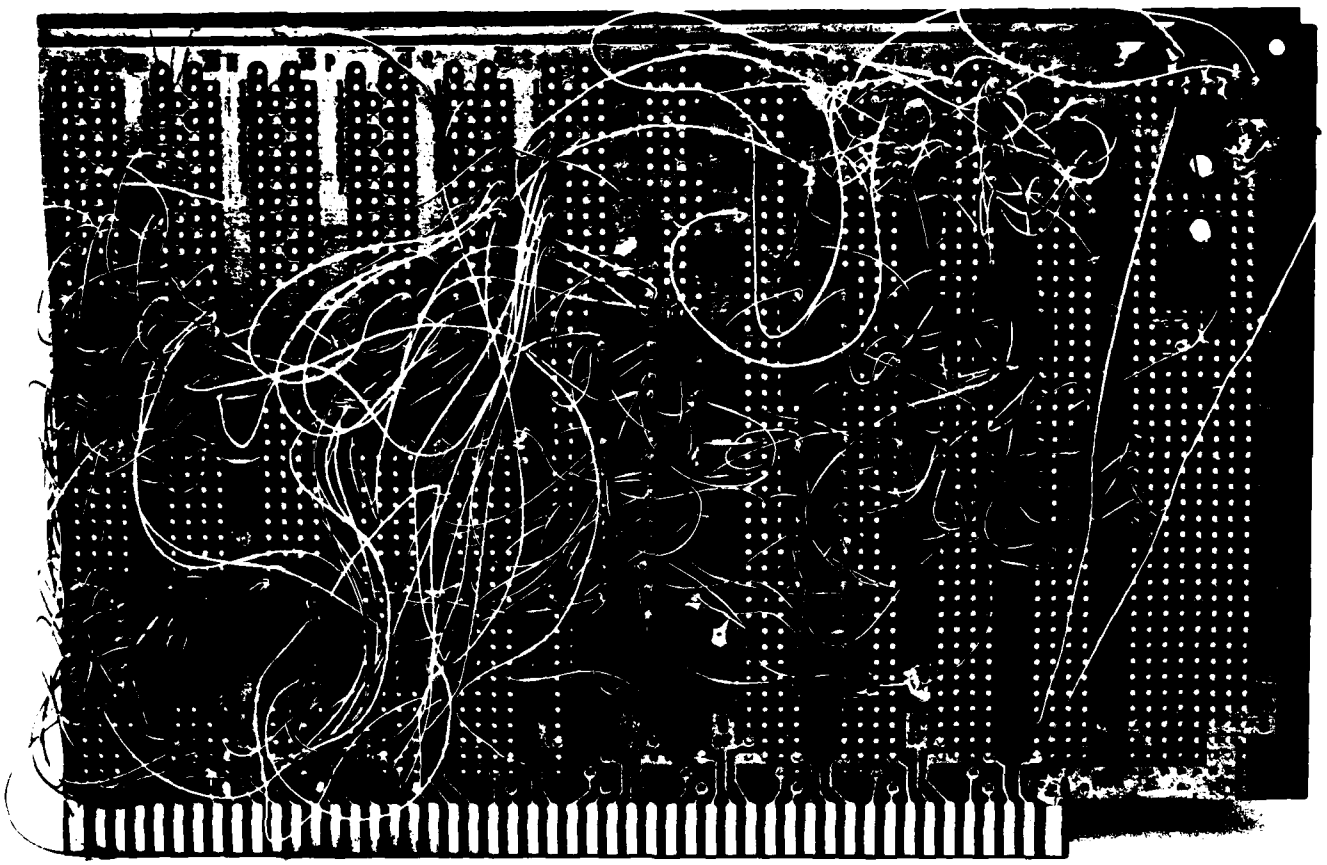


FIGURE 23. STIMULATORS: WIRING SIDE

IV. Experimental Procedure and Data

In order to test the combined operation of the computer hardware, software, feedback channels and stimulators, surgery was done. Then the feedback channels and stimulators were connected. Finally, the computer hadware and software were run in order to produce the isometric contraction. Each of these steps are discussed in detail in the following sections:

Initial Surgery

Animals used in the experiment were female adult cats weighing between two and four kg. Each animal was fasted for at least twelve hours before surgery. Initially, each animal was injected with α-chloralese at the rate of 55 mg./kg and given supplemental doses throughout the experiment via the jugular cannula. A heating pad placed between the animal and the operating table regulated the animals core temperature at 38°C. Vital signs of the animal were electronically monitored and recorded for the duration of the experimentation.

The animal was first placed on the table in the prone position. Steel pins locked the rear left leg into place by being driven into the knee and ankle joints. Next, an incision was made from the sacral plexis to just above the ankle on the locked leg. By opening the incision, the medial head of the gastrocnemius muscle was exposed. The gastrocnemius was then solely exposed by clearing out the surrounding fatty tissue and muscles.

With the muscle thus exposed, the next task was to remove the lower end of the muscle from the leg. This was done by first cutting away all muscles attached to the calcaneous and then removing the calcaneous from the leg bone. The now free end of muscle attached to the calcaneous was tied to the

stainless steel tension transducer bar and stretched by motor until maximum tension was obtained when stimulated to tetanis. During the time the muscle was exposed, heat of the tissue was maintained at 38°C by use of a 150 watt heat lamp.

Muscles were stimulated directly through the siatic nerve. The nerve was divided into three equal bundles such that stimulation of each bundle would cause the muscle to develop the same contraction strength. While the nerve was exposed it was kept electrically isolated and viable by immersion in a liquid parafin and dura matter bath.

During the experiment, each bundle was implanted with one of the three stimulator electrodes. The three bundles were then sequentially stimulated by the three electode pairs as described in the procedures section below. Therefore the motor units were recruited and the stimulation could be be observed by the muscle contraction.

Experimental Procedure

The object of the experimentation was to observe how accurately the computer could maintain an isometric contraction of the gastrocnemius muscle through the point of muscle fatigue. Once the animal was ready for experimentation, with the gastrocnemius exposed, the stimulator was attached to the sciatic nerve via an isolation box. This box provided isolation of the stimulator channels from one another, as well as isolation from any transient noise signals. The feedback from the strain gauge bridge was first amplified with an operational amplifier with a gain of 33. This adjusted the output of the strain gauge bridge so that a variance from zero to five volts was obtained for input to the analog to digital converter.

The next step in the procedure was to initialize the computer and then fire the muscle at a tetanising frequency ($100H_z$) to determine the maximum tension developed. As the muscle contracted away from the steel tension transducer bar, the maximum tension was noted. From this maximum tension, the target target for the isometric contractions was determined. The first target would be 40% of the maximum, the second 70% of the maximum and the last 25% of the maximum tension. Once the target tension was determined, the target set potentiometer was adjusted to the appropriate value. This in turn set the output of the first analog to digital convertor to the correct digitized target for each contraction.

After the target set output was correctly adjusted, stimulation was started. Initially, the frequency of stimulation was set for approximately 10Hz. The pulse duration of each stimulator pulse was chosen to be 100 micro-seconds as current literature indicated the maximum latitude in developed tension with respect to stimulation voltage occurred at this pulse width (Petrofsky, 1978: 305).

Data

Computer controlled stimulation was not completed as the stimulator outputs were not operating within the correct frequency range. Therefore, the data from the experiment was derived from the literature and a close approximation of the output data can be modeled as shown in Figure 49 (Petrofsky; 1978).

Figure 49 demonstrates the predicted results in the tension exerted upon the steel tension bar by the gastrocnemius as a function of the percentage of desired tension and the firing rate

of the stimulators. As the muscle fatigues denoted by the horizontal axis, the computer has little trouble maintaining the strength of the contraction until all motor units are recruited. After all motor units are recruited and the exerted tension on the bar drops, the frequency of the stimulation can be seen slowly increasing to maintain the isometric contraction. After the stimulation frequency passes the tetanizing frequency, 46 Hz, the stimulation was completed and the muscle was deened fatigued. By increasing the frequency of the stimulation, it can be seen that an almost 30 percent increase in the fatigue was obtained over no increase in frequency.

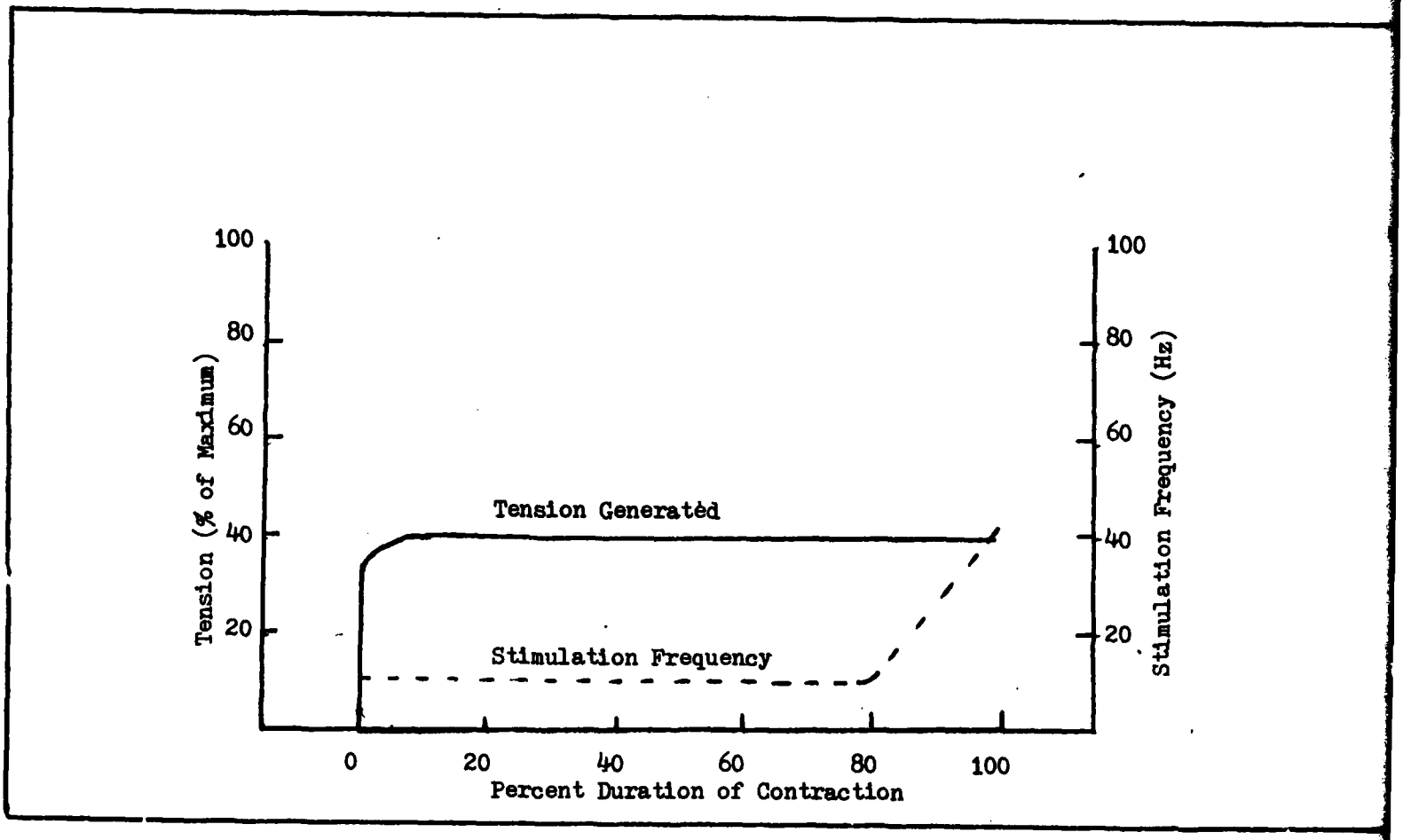


FIGURE 24. EXPECTED RESULTS

V. Conclusions

The approach to complete the objectives outlined was followed as outlined at the beginning of this project. The state-of-the-art 8085 microprocessor was constructed and tested for proper functioning by running related programs through the computer system. The actual programming for the experimentation could not be tested as the stimulators could not be debugged for proper functioning. However, the computer system was built based on original designs by the author and proven to be a functioning unit.

The analog to digital feedback channels were tested via hardware testing to ensure that proper functioning was achieved. Mounted on an S-100 edge card, the analog to digital converters did function even though the required interface to the computer system could not be executed due to erroneous timing signals. If in fact the timing signals to the analog to digital channels were corrected, then the entire feedback loop would be ready for operation in the stimulation of gastrocnemius.

Each digital to analog channel was first sucessfully tested through hardware testing. Then each channel was mounted on the S-100 edge connector card with the analog tc digital channels. For the same reason, the digital to analog channels that were to control the stimulators could not be interfaced with the microprocessor. Again, if the timing error between the microprocessor system and the digital to analog channels was corrected the control of the stimulator would be complete.

Two channels of stimulators were constructed, each emitting three

sequential pulses of amplitude five volts. Two channels of stimulators were constructed to allow future testing of dynamic muscle contractions. In essence, dynamic muscle testing would enable follow-on researchers to examine limb movement around a joint by stimulating a pair of opposing muscles. Eventually when enough data is collected on the testing the dynamic control of limbs, the root of the paraplegic problem will have been addressed. The possibility for co-ordinated movement such as walking or bycycling is then, therefore,in the foreseeable future.

As far as the project is concerned, enough data was gathered to determine that the state-of-the-art computer system will be quick enough for dynamic testing of at least one pair of muscles, if not more. The microprocessor has also been recently (1980) manufactured to run at a clock speed of five MHz, making it two and one-half times as quick as the original 8080 technology used in the initial experimentation. Since this new product is directly pin compatible with the 8085 used in this project, it could feasibly be "plugged" in to the existing system with no changes in software and minor changes in the hard ware. These minor changes would be only in varying of the 8080 compatible timing signals. Once these changes are made a new faster system could be made from the working, existing one.

Although no data was collected as far actual experimentation on an anesthetized animal, work will still be done to complete the project. After ironing out the timing problem that has plagued the project since its inception, a completely working system would result and the experimentation as outlined in the experimental procedures section

could be accomplished. The experimentation will be carried out at Wright State University, with the projected result tom be identical to the predicted result of the project as outlined in the data section of the report. If successful results are obtained, dynamic testing of the new system will ensue as only very minor changes in the programming are needed.

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Appendix A

Calculation of the timing signal pulse widths and points of occurrence took into consideration many specifications. The clock and Ale signals from the 8085 were the only signals that could be used to create the 8080 timing signals; ϕ_1, ϕ_2 and Psync. The time of occurrence and pulse width for each signal was then calculated for the 8085 by multiplying the values of the 8080 signals by a reducing constant The values are shown in thetable below.

Signal	8080 Time of Occurrence	8080 Pulse Width	8085 Time of Occurrence	8085 Pulse Width
ϕ_1	0 ns	106 ns	0 ns	74 ns
ϕ_2	120 ns	220 ns	83 ns	163 ns
PSYNC	140 ns	480 ns	97 ns	333 ns

As shown in Figure 9a. , the ϕ_1 signal is triggered from the falling edge of the 8085 clock output. The values for the capacitors and timing resistors for the ϕ_1 signal as shown in Figure 9b, are 17 pF and 7.5 kΩ respectively. The falling edge of the ϕ_1 signal was used to drive the leading edge of the ϕ_2 signal as shown in Figure 9b. The values for the timing components for the ϕ_2 signal are 78 pF and 5 KΩ. The Falling edge of the 8085 Ale signal was used to trigger the rising edge of the Psync signal. The timing components needed to make the Psync pulse equal to one clock cycle were a 100 pF capacitor and a 9 K resistor.

Vita

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Increasing numbers of spinal cord injury victims due to automobile accidents, sports injuries and gunshot wounds reflect a growing need for a paralysis cure. One method under study to alleviate the plight of spinal cord injury victims is the use of microcomputers to control the stimulation of the remaining motor nerve.. If the motor nerve is intact and is carefully stimulated, muscle contraction will occur. Coordinated movement of two or more opposing muscles can produce limb movement and using small, fast

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microcomputers to control the stimulation of the muscle tissue, and hence movement, a possible cure to the paraplegic problem may be found.

The object of this project was to produce contolled fatiguing muscle contractions in the gastrocnemius muscle of cats. The composition of the muscle tissue is identical to man's and controlled contractions in the cat muscle will lead to the same contractions in man. In order to produce an accurately controlled contraction, first a computer system was constructed from an Intel 8085 microprocessor. Next, controllable stimulators for the motor nerves were constructed and controlled by the microprocessor via digital to analog convertors. Feedback from the muscle under test was then interpreted through analog to digital convertors, such that the microprocessor controlled the contraction tension of the muscle as a constant. Through the feedback, the processor was able to produce highly accurate sustained muscle contractions and with the high speed of the system, future multi-muscle control systems could develop. This would allow movement in previously unusable limbs and pave the way for future solutions to the paraplegic problem.